1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		356292	PRODUCTION RELEASED	12/17/04	?

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9	INTREPID MEMORY INTERFACE/BOOTROM
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11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
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22	M11 POWER

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25	MMM & BATTERY CURRENT SENSE CIRCUIT
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SCHEM,MLB,PB15"
12/17/2004

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EMI
GPU_SS	EXT_TMDS (BETTER/BEST)
VGA_BUFFER_RES	INT_TMDS (BEST128)
MMM	SUPERCAP
INT_TMDS (BETTER/BEST)	ADT7460
EXT_TMDS (BEST128)	
BACKUP_BATT	
ADT7467	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6680	1	SCHEM,MLB,PB15	SCH1	
820-1679	1	PCBF,MLB,PB15	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

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TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6680 REV. A

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U51 INTREPID

J23 Ethernet Connector P.28
4 DATA PAIRS
U43 Ethernet PHY P.28
G/MII 3.3V 10/100/1000 8BIT TX 8BIT RX 125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHZ
J20 FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
U36 FireWire PHY P.29
1394 OHCI 3.3V 8BIT TX/RX 50MHZ

J13 ODD Connector P.26
EIDE
J12 HDD Connector P.26
UIDE

J15 SW MODEM Connector P.27
J3 LIO/Audio Connector P.27
I2S
I2C
I2C
U53/J1/J18 Fan Circuit P.27

J2 RUX Board Connector P.24
J19 ALS BOARD Connector P.24
J16 BACKUP BATTERY CONNECTOR P.33
C692 SUPERCAP P.33
J26 Battery Connector P.32
Power Supply & Charger P.32-36
J27 DC-In Connector P.32
J8 SLEEP LED P.24
SMBUS 3.3V

U15/U20/U58 MMM P.25
U41 BATTERY CURRENT SENSOR P.25

NOT USED

ETHERNET 10/100/1000 P.13	FIREWIRE 400 MB/S P.13	UATA 100 P.13	EIDE P.13	CARDSLOT P.13	I2S P.14	I2C P.13 P.14

NOT USED USB PORT A P.14
NOT USED USB PORT B P.14
NOT USED USB PORT C P.14
NOT USED USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8

SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12

J28 Serial Debug Connector P.27
U28 PMU P.31
SERIAL 5V
J5 CARDBUS Connector P.18
33MHZ 16/32 BITS 3.3V/5V
U8 TI PCI1510 CardBus Controller P.18
U11 BOOT ROM 1M X 8 P.9
J6 AIRPORT Connector P.26
PCI BUS 32BITS 33MHZ 3.3V

J3 BlueTooth (LIO) P.27
J10 SPIDEY P.24
MAXBUS 1.8V 167MHZ 32BIT ADDRESS 64BIT DATA

AGP BUS 1.5V/3.3V 32BITS 66MHZ
U47 ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

U17 NEC USB2.0 EHCI HC P.17
J3 LEFT USB (VIA LIO) P.27
J17 RIGHT USB (VIA STATLER) P.27

U56 APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU

DDR MEMORY P.9
MEMORY BUS 2.5V 167MHZ 64BITS
U16/U18/U28/U27 2:1 DDR MUXES P.10
J25 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11

J4 Inverter Connector P.23
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14 LCD Panel Connector P.23
J21 S-Video Connector P.23
J22 DVI-I Connector P.23

SYSTEM BLOCK DIAGRAM

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POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 32

INRUSH LIMITER PG 32

+24V_PBUS

1V20_REF - PG 33
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS
BUCK VCC REGULATOR (LTC1625) PG 33
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 33

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 34

VCC
STBYMD
PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 33

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 32

+BATT

3S 2P 18650 CELLS

DC/DC (LTC3411)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 36

+1.8V_MAIN
MAXBUS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 32

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 36

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V
ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER

+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN

INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)

SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK
D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

DCDC_EN
SLEEP

MAXBUS SEQUENCING

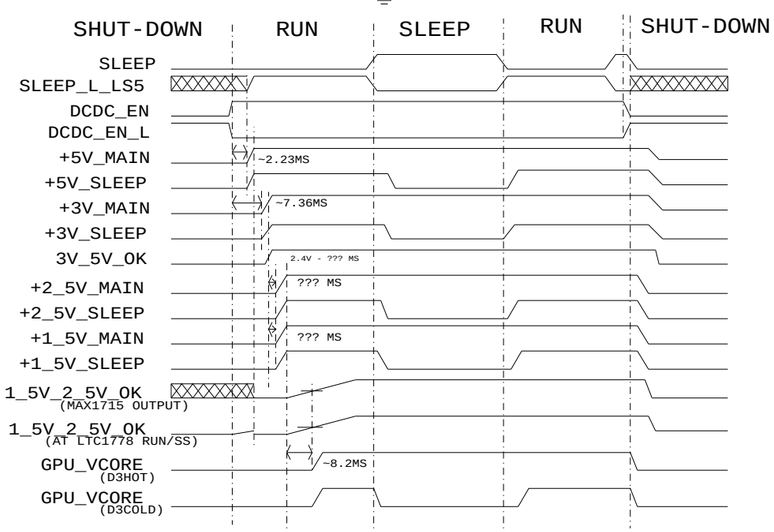
+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 35

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
3	PREPREG (3 MIL)	GROUND (1/2 OZ)
4	CORE (3 MIL)	SIGNAL (1/2 OZ)
5	PREPREG (5 MIL)	CUT POWER PLANE (1 OZ)
6	CORE (5 MIL)	CUT POWER PLANE (1 OZ)
7	PREPREG (5 MIL)	SIGNAL (1/2 OZ)
8	CORE (3 MIL)	GROUND (1/2 OZ)
9	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3 MIL)	SIGNAL (1/2 OZ + COPPER PLATING)

BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS
ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA
ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER
SH1 QG-583040 SHLD-SM — CHGND3

MECH. HOLES
ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301 SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302 SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10 SPN NO_TEST=TRUE

GROUND VIAS

ZT76 ZT28 ZT72 ZT69 ZT68 ZT64 ZT61 ZT38 ZT39 ZT40 ZT41 ZT46 ZT71 ZT78 ZT80
ZT50 ZT51 ZT52 ZT53 ZT57 ZT60 ZT82 ZT22 ZT17 ZT35 ZT45 ZT79 ZT81 ZT83 ZT49
ZT48 ZT47 ZT54 ZT55 ZT56 ZT84 ZT5 ZT15 ZT44 ZT4 ZT8 ZT6 ZT32 ZT3 ZT10
ZT11 ZT34 ZT20 ZT43 ZT70 ZT2 ZT9 ZT75 ZT73 ZT63 ZT77 ZT66 ZT62 ZT65 ZT13
ZT25 ZT19 ZT24 ZT67 ZT37 ZT29 ZT31 ZT1 ZT14 ZT12 ZT27 ZT26 ZT30 ZT33 ZT18

All: HOLE-VIA-20R10

BOARD INFORMATION

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D	051-6680	A
SCALE: NONE	SHT 4 OF 46	

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CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 6 35 40 41

R38 470 5% 1/16W MF 402

C32 10uF 20% 6.3V CERM 805 | C59 10uF 20% 6.3V CERM 805 | C104 10uF 20% 6.3V CERM 805
C33 10uF 20% 6.3V CERM 805 | C58 10uF 20% 6.3V CERM 805 | C107 0.1uF 20% 10V CERM 402
C34 2.2uF 20% 10V CERM 805 | C62 2.2uF 20% 10V CERM 805 | C109 0.1uF 20% 10V CERM 402

C26 0.1uF 20% 10V CERM 402 | C39 0.1uF 20% 10V CERM 402 | C50 0.1uF 20% 10V CERM 402 | C45 0.1uF 20% 10V CERM 402 | C29 0.1uF 20% 10V CERM 402 | C55 0.1uF 20% 10V CERM 402 | C2 0.1uF 20% 10V CERM 402 | C108 0.1uF 20% 10V CERM 402
C30 0.1uF 20% 10V CERM 402 | C49 0.1uF 20% 10V CERM 402 | C31 0.1uF 20% 10V CERM 402 | C47 0.1uF 20% 10V CERM 402 | C27 0.1uF 20% 10V CERM 402 | C53 0.1uF 20% 10V CERM 402 | C103 0.1uF 20% 10V CERM 402 | C110 0.1uF 20% 10V CERM 402
C28 0.1uF 20% 10V CERM 402 | C48 0.1uF 20% 10V CERM 402 | C56 0.1uF 20% 10V CERM 402 | C46 0.1uF 20% 10V CERM 402 | C25 0.1uF 20% 10V CERM 402 | C54 0.1uF 20% 10V CERM 402 | C68 0.1uF 20% 10V CERM 402 | C1 0.1uF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)

OMIT
XW34
SM

27 ADT7467_VCORE_MON 1 2

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 6 7 8 15 16 35 40

R89 470 5% 1/16W MF 402

C38 0.1uF 20% 10V CERM 402 | C88 0.1uF 20% 10V CERM 402 | C44 0.1uF 20% 10V CERM 402 | C20 0.1uF 20% 10V CERM 402 | C87 0.1uF 20% 10V CERM 402 | C61 0.1uF 20% 10V CERM 402
C18 0.1uF 20% 10V CERM 402 | C89 0.1uF 20% 10V CERM 402 | C72 0.1uF 20% 10V CERM 402 | C10 0.1uF 20% 10V CERM 402 | C69 0.1uF 20% 10V CERM 402 | C81 0.1uF 20% 10V CERM 402
C86 0.1uF 20% 10V CERM 402 | C9 0.1uF 20% 10V CERM 402 | C75 0.1uF 20% 10V CERM 402 | C73 0.1uF 20% 10V CERM 402 | C17 0.1uF 20% 10V CERM 402 | C82 0.1uF 20% 10V CERM 402

40 CPU_AVDD

C810 0.1uF 20% 10V CERM 402 | C811 4.7uF 20% 6.3V CERM 805

+3V_SLEEP

VDD | OVDD | AVDD | OVDDSENSE

(NAP VOLTAGE=0.98V FOR ALL CONFIG.)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2952	1	IC,A7PM,R1.2.3,1.50GHZ,1.2VCORE,18W,85C	U56	CRITICAL	CPU_BTR
337S2953	1	IC,A7PM,R1.2.3,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST
337S3069	1	IC,A7PM,R1.2.3,1.67GHZ,1.26VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE126
337S3027	1	IC,A7PM,R1.3,1.50GHZ,1.20VCORE,18W,85C	U56	CRITICAL	NO STUFF
337S3028	1	IC,A7PM,R1.3,1.67GHZ,1.29VCORE,18W,85C	U56	CRITICAL	NO STUFF

OMIT
U56
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

38 CPU_BR_L D2 BR*
38 CPU_BG_L M1 BG*
38 CPU_TS_L L4 TS*
5 CPU_PULLDOWN E11 A0
H1 A1
C11 A2
G3 A3
38 CPU_ADDR<0> F10 A4
38 CPU_ADDR<1> L2 A5
38 CPU_ADDR<2> D11 A6
38 CPU_ADDR<3> D1 A7
38 CPU_ADDR<4> C10 A8
38 CPU_ADDR<5> G2 A9
38 CPU_ADDR<6> D12 A10
38 CPU_ADDR<7> L3 A11
38 CPU_ADDR<8> G4 A12
38 CPU_ADDR<9> T2 A13
38 CPU_ADDR<10> F4 A14
38 CPU_ADDR<11> V1 A15
38 CPU_ADDR<12> J4 A16
38 CPU_ADDR<13> R2 A17
38 CPU_ADDR<14> K5 A18
38 CPU_ADDR<15> W2 A19
38 CPU_ADDR<16> J2 A20
38 CPU_ADDR<17> K4 A21
38 CPU_ADDR<18> N4 A22
38 CPU_ADDR<19> J3 A23
38 CPU_ADDR<20> M5 A24
38 CPU_ADDR<21> P5 A25
38 CPU_ADDR<22> N3 A26
38 CPU_ADDR<23> T1 A27
38 CPU_ADDR<24> V2 A28
38 CPU_ADDR<25> U1 A29
38 CPU_ADDR<26> N5 A30
38 CPU_ADDR<27> W1 A31
38 CPU_ADDR<28> B12 A32
38 CPU_ADDR<29> C4 A33
38 CPU_ADDR<30> G10 A34
38 CPU_ADDR<31> B11 A35

NC C1 AP0
NC E3 AP1
NC H6 AP2
NC F5 AP3
NC G7 AP4

38 CPU_TT<0> E5 TT0
38 CPU_TT<1> E6 TT1
38 CPU_TT<2> F6 TT2
38 CPU_TT<3> E9 TT3
38 CPU_TT<4> C5 TT4
38 CPU_TBST_L F11 TBST*
38 CPU_TSIZ<0> G8 TSIZ0
38 CPU_TSIZ<1> F7 TSIZ1
38 CPU_TSIZ<2> E7 TSIZ2
38 CPU_GBL_L E2 GBL*
38 CPU_WT_L D3 WT*
38 CPU_CI_L J1 CI*
38 CPU_AACK_L R1 AACK*
38 CPU_ARTRY_L N2 ARTRY*
5 CPU_SHD0_L E4 SHD0*
5 CPU_SHD1_L H5 SHD1*
38 CPU_HIT_L B2 HIT*

GND

BVSEL B7 CPU_BUS_VSEL 7
SYSCLK A10 SYSCLK_CPU 8 37
CLK_OUT H2 CPU_CLKOUT_SPN NO_TEST=TRUE
PLL_CFG0 B8 CPU_PLL_CFG<0> 7
PLL_CFG1 C8 CPU_PLL_CFG<1> 7
PLL_CFG2 C7 CPU_PLL_CFG<2> 7
PLL_CFG3 D7 CPU_PLL_CFG<3> 7
PLL_CFG4 A7 CPU_PLL_CFG<4> 7
DBG* M2 CPU_DBG_L 8 38
DRDY* R3 CPU_DRDY_L 8 38
DTI0 G1 CPU_EDTI 5
DTI1 K1 CPU_DTI<0> 8 38
DTI2 P1 CPU_DTI<1> 8 38
DTI3 N1 CPU_DTI<2> 8 38

TDI B9 JTAG_CPU_TDI 5 6 41
TDO A4 JTAG_CPU_TDO_TP 41
TMS F1 JTAG_CPU_TMS 5 6 41
TCK C6 JTAG_CPU_TCK 5 6 41
TRST* A5 JTAG_CPU_TRST_L 6 41
LSSD_MODE* E8 CPU_LSSD_MODE 5
L1_TSTCLK G8 CPU_L1TSTCLK 5
L2_TSTCLK B3 CPU_L2TSTCLK 5

TA* K6 CPU_TA_L 8 38
TEA* L1 CPU_TEA_L 8 38

TBEN E1 CPU_TBEN 5 8
QREQ* P4 CPU_QREQ_L 8 38
QACK* G5 CPU_QACK_L 8 38
CKSTP_IN* A3
CKSTP_OUT* B1 CPU_CHKSTP_OUT_L 5 41

INT* D4 MPIC_CPU_INT_L 5 14
SMI* F9 CPU_SMI_L 5 31
MCP* C9 CPU_MCP_L 5
SRESET* A2 CPU_SRESET_L 5 41
HRESET* D8 CPU_HRESET_L 5 6 7 41

PMON_IN* D9 CPU_PMONIN_L 5
PMON_OUT* A9 NC

BMODE0* G9 CPU_EMODE0_L 7
BMODE1* F8 CPU_EMODE1_L 5

EXT_QUAL A11 CPU_PULLDOWN 5
CHKS* A12 CPU_CHKS_L 5
SRW0* B10
SRW1* E10 CPU_SRWX_L 5
IARTRY0* B6 CPU_PULLUP 5
DX* D10 CPU_PULLDOWN 5

CPU INTERNAL PLL FILTERING

For CPU DFS mode, Must stuff R748
NO STUFF

R453 10 1% 1/16W MF 402 — CPU_VCORE_SLEEP 5 6 35 40 41
R748 10 1% 1/16W MF 402 — 40 CPU_AVDD_VOUT

Vout=0.59*(1+R1/R2)
Place R449 & R452 close to U5 pin 6&5

R302 0 5% 1/16W MF 603

U5
FAN2558
SOT23-6
VIN 1 | PG 4 | EN 3 | GND 2 | VOUT 6 | ADJ 5

C626 0.001uF 10% 50V CERM 402
R449 118K 1% 1/16W MF 402
C102 1uF 10% 6.3V CERM 402
R452 100K 1% 1/16W MF 402

40 CPU_AVDD_VIN
CPU_AVDD_SHDN_L
CPU_AVDD_ADJ

D17 SN MBR0530
R455 100K 5% 1/16W MF 402
C85 2.2uF 10% 6.3V CERM1 603
C502 0.1uF 20% 10V CERM 402

35 VCORE_SHDN_L
VCORE_SHDN_L_3V

R755 0 5% 1/16W MF 402 — 470OHM FOR BOOT BANGER
R775 200K 5% 1/16W MF 402 — NO STUFF — 470OHM FOR BOOT BANGER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0413	1	RES,MF,1/16W,105K OHM,1%,0402,SMD	R449 (R1)		CPU_BTR
114S1155	1	RES,MF,1/16W,115K OHM,1%,0402,SMD	R449 (R1)		CPU_BST_VCORE126

+1_5V_SLEEP — R281 0 5% 1/16W MF 603 — 1_5V_MAXBUS
+1_8V_SLEEP — R283 0 5% 1/16W MF 603 — 1_8V_MAXBUS

40 35 16 15 8 7 6 5 MAXBUS_SLEEP

MPC7447 PULL-UPS

5 CPU_TBEN — R24 10K 5% 1/16W MF 402
5 CPU_CHKS_L — R4 10K 5% 1/16W MF 402
5 CPU_SHD0_L — R25 10K 5% 1/16W MF 402
5 CPU_SHD1_L — R46 10K 5% 1/16W MF 402
5 CPU_MCP_L — R13 10K 5% 1/16W MF 402
5 CPU_LSSD_MODE — R26 10K 5% 1/16W MF 402
5 CPU_L2TSTCLK — R8 10K 5% 1/16W MF 402
41 5 CPU_CHKSTP_OUT_L — R7 1K 5% 1/16W MF 402
5 CPU_SRWX_L — R28 10K 5% 1/16W MF 402
5 CPU_PMONIN_L — R27 10K 5% 1/16W MF 402
5 CPU_EMODE1_L — R33 10K 5% 1/16W MF 402
5 CPU_PULLUP — R3 1K 5% 1/16W MF 402
41 7 6 5 CPU_HRESET_L — R20 10K 5% 1/16W MF 402
31 5 CPU_SMI_L — R34 10K 5% 1/16W MF 402
41 6 5 JTAG_CPU_TMS — R32 470 5% 1/16W MF 402
41 6 5 JTAG_CPU_TDI — R2 470 5% 1/16W MF 402
14 5 MPIC_CPU_INT_L — R19 10K 5% 1/16W MF 402
41 5 CPU_SRESET_L — R6 10K 5% 1/16W MF 402

5 CPU_L1TSTCLK — R37 10K 5% 1/16W MF 402
5 CPU_EDTI — R36 10K 5% 1/16W MF 402
41 6 5 JTAG_CPU_TCK — R11 10K 5% 1/16W MF 402
5 CPU_PULLDOWN — R45 470 5% 1/16W MF 402

MPC7447 MAXBUS

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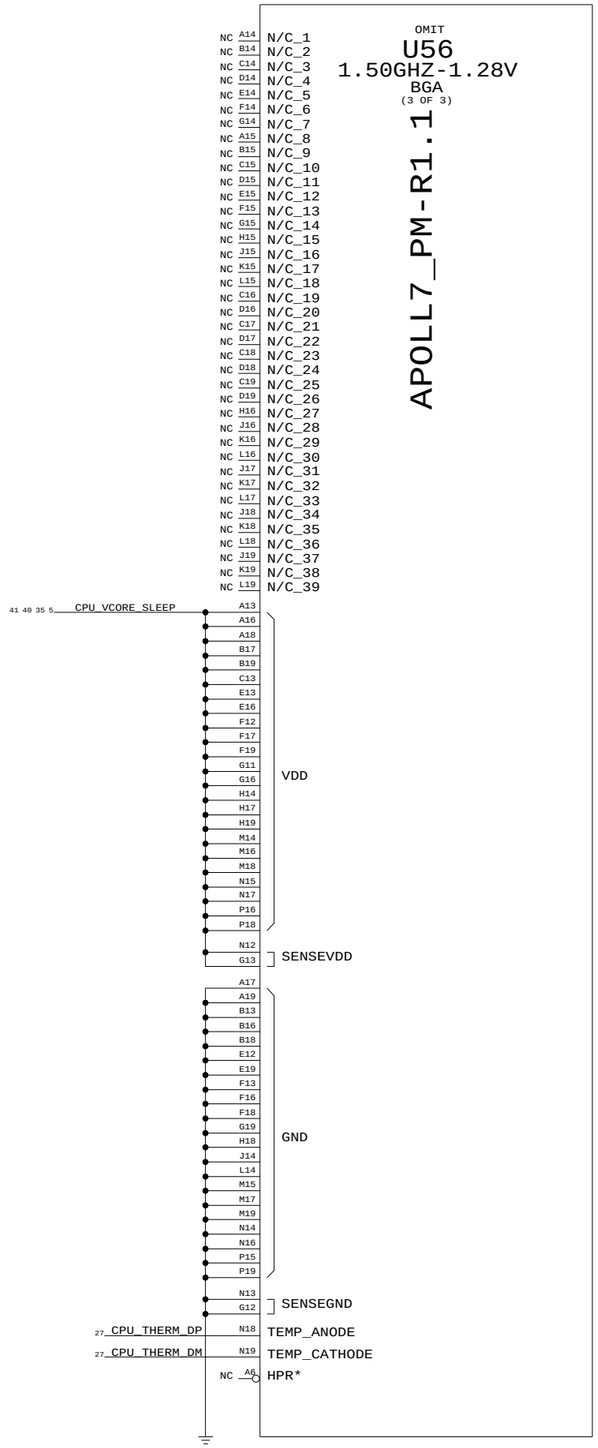
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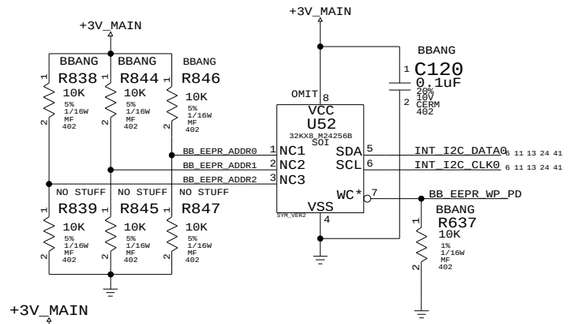
SIZE D | DRAWING NUMBER 051-6680 | REV. A
SCALE NONE | SHT 5 OF 46

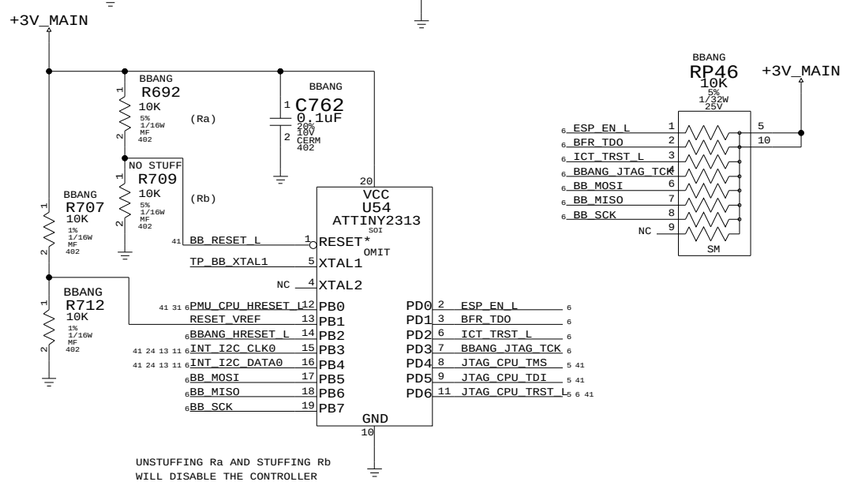
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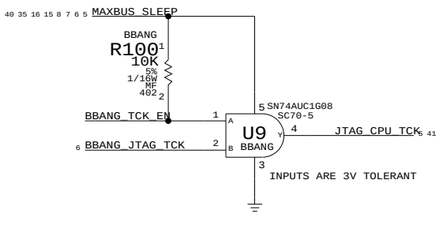
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

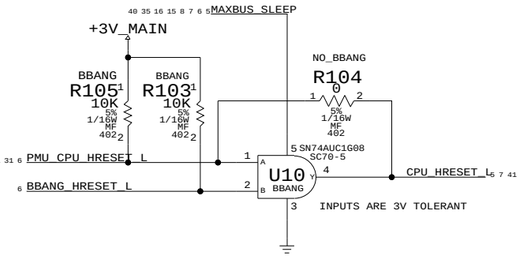


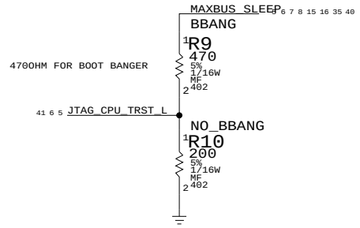


UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BBANGER	U54	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BBANGER	U52	BBANG







MPC7447/BBANG

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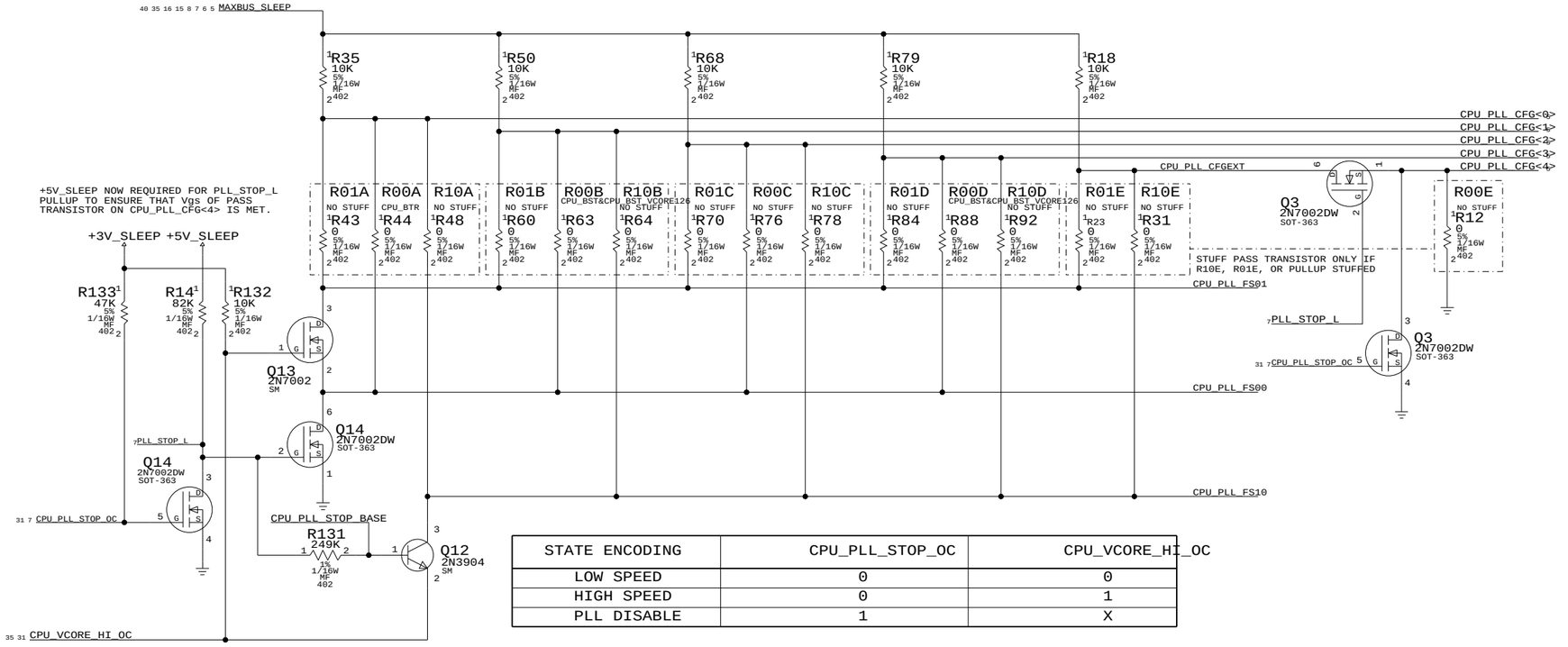
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 6 OF 46	

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CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

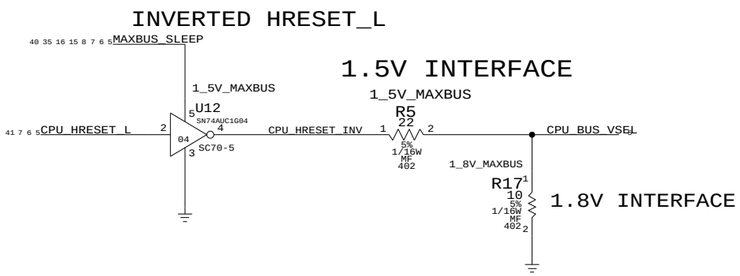
CPU FREQUENCY CONFIGURATION

APOLLO 7PM

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

CPU CONFIGURATION

MAXBUS VSEL



BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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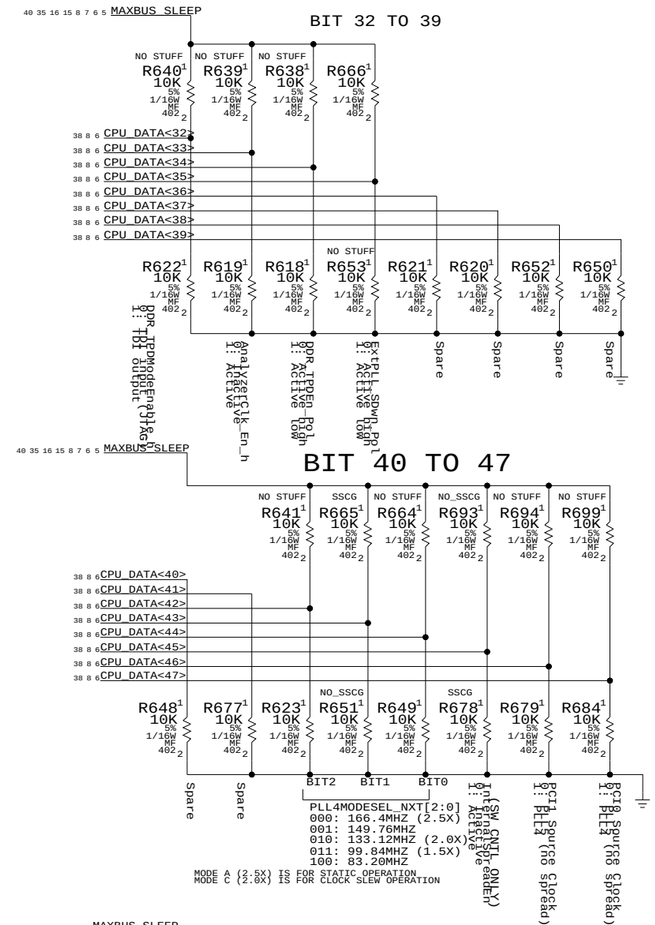
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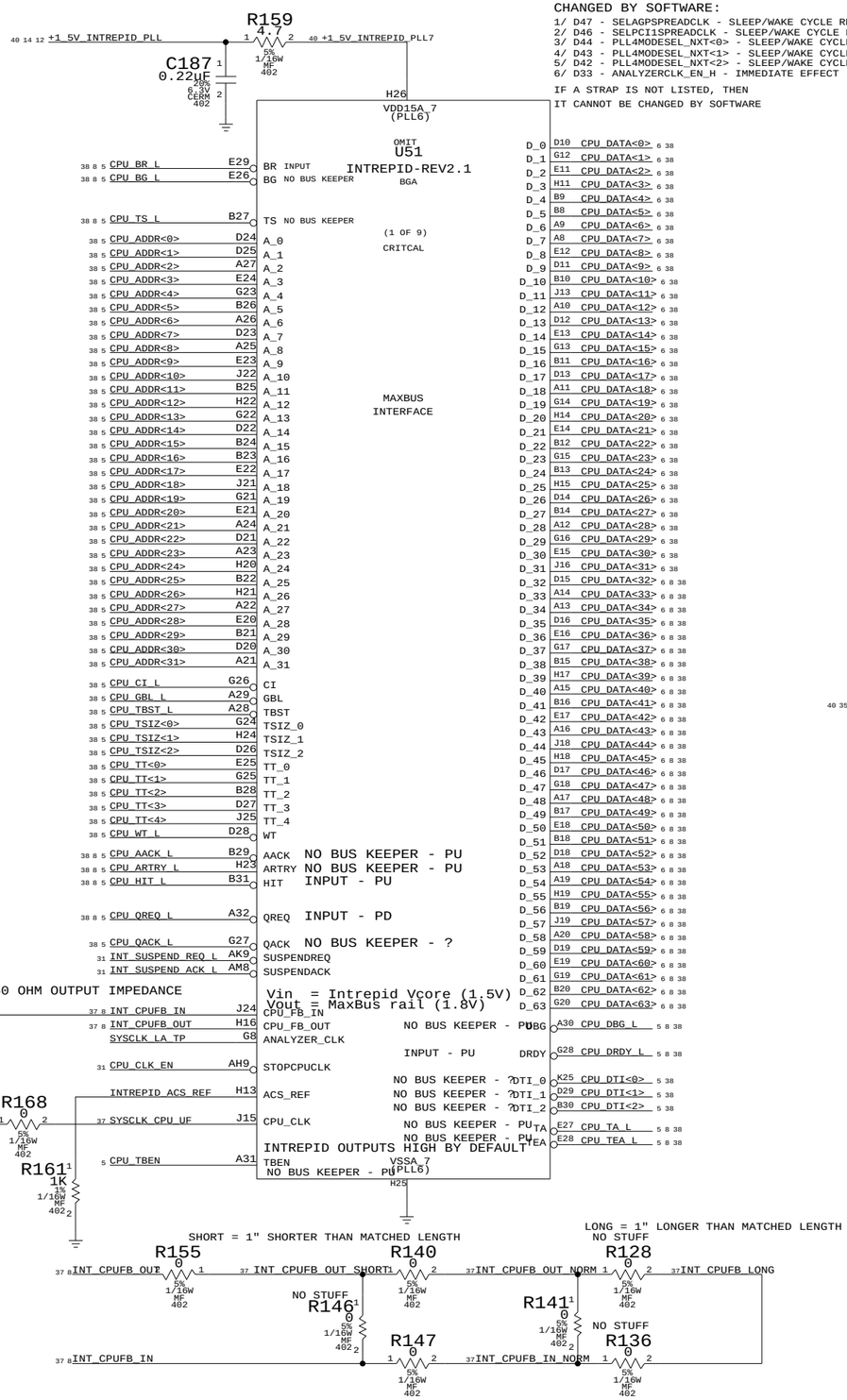
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SIZE D | DRAWING NUMBER 051-6680 | REV. A

SCALE NONE | SHT 7 OF 46

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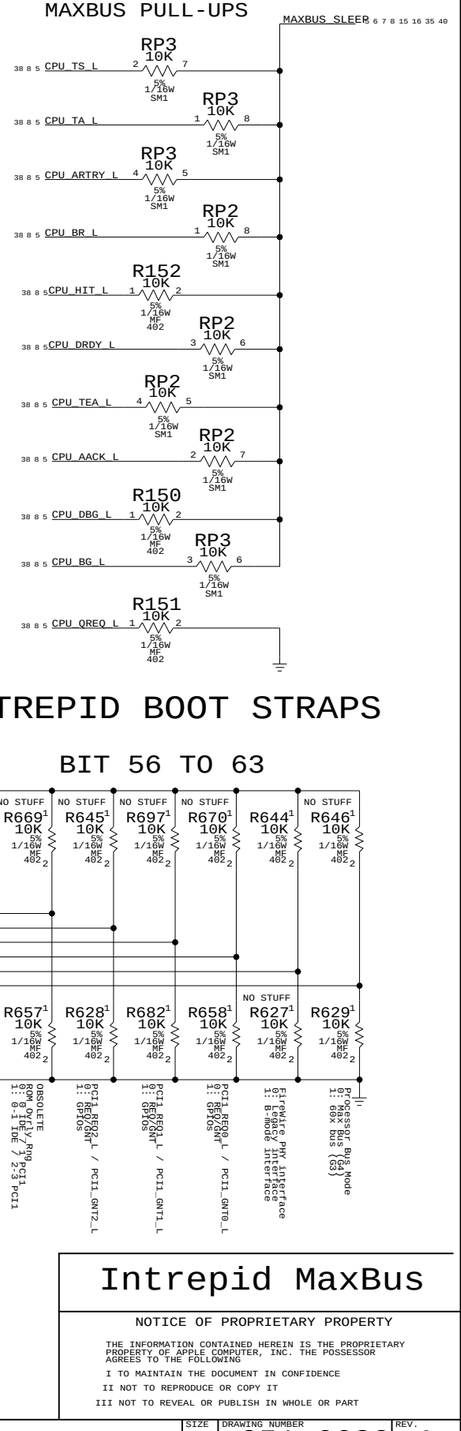




THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE



Intrepid MaxBus

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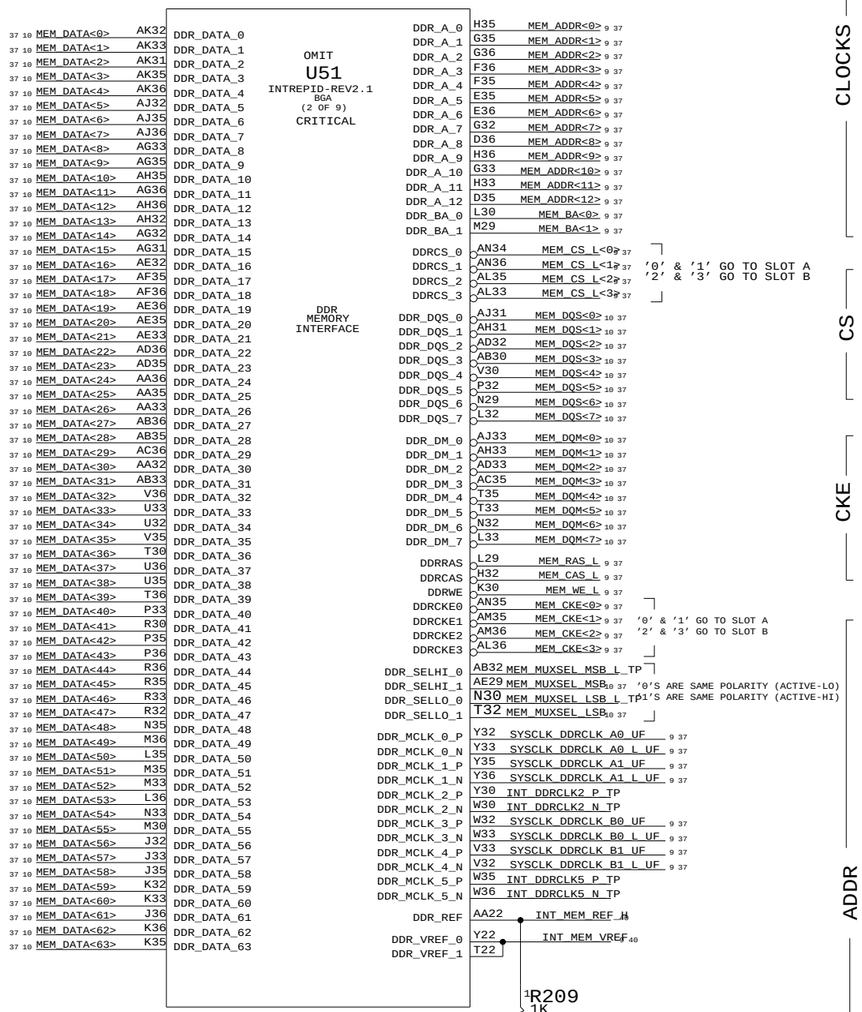
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 8 OF 46	

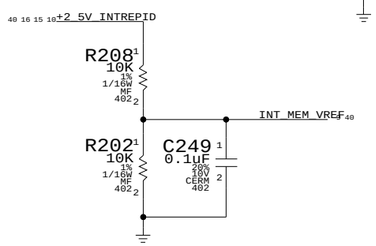
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SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

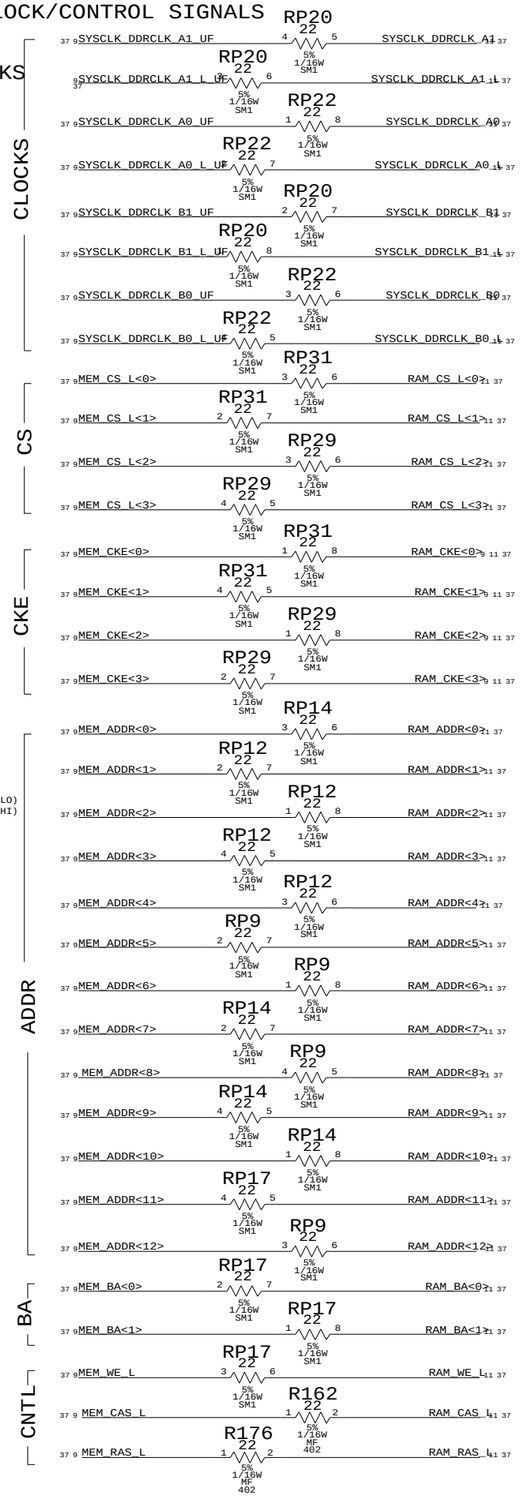
PINS ARE SWAPABLE FOR RPAKS



MEM_VREF



CLOCKS



CS

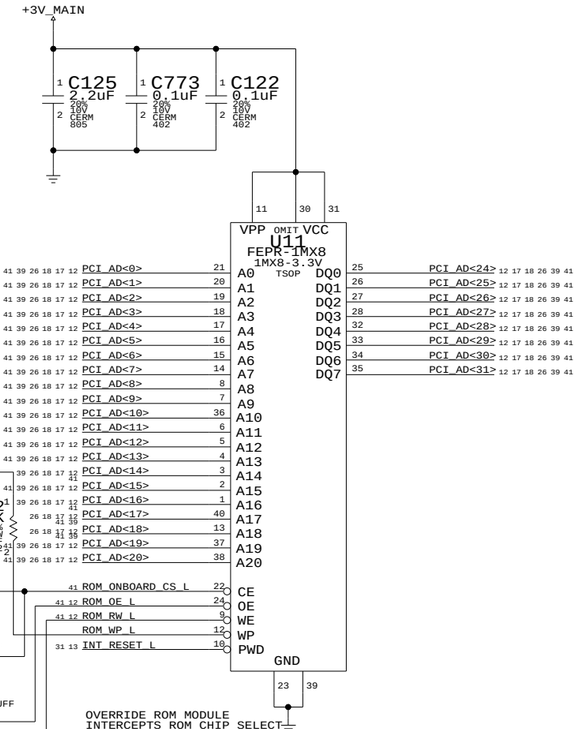
CKE

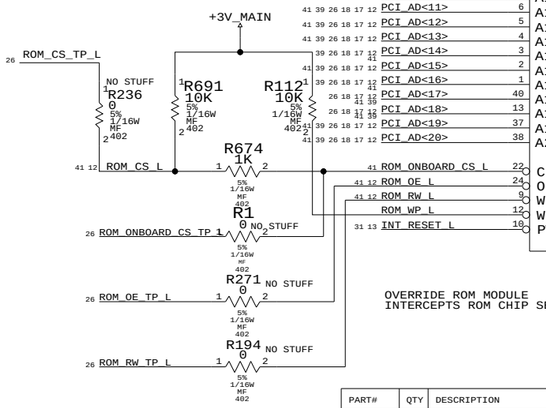
ADDR

BA

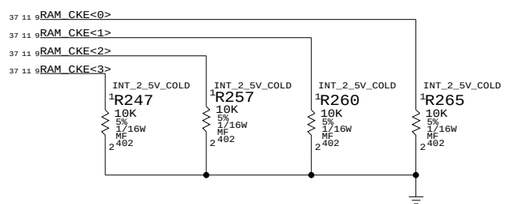
CNTL

1MB BOOT ROM





Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1555	1	IC,BOOTROM Q16B	U11	CRITICAL	?

INT - DDR/BOOTROM

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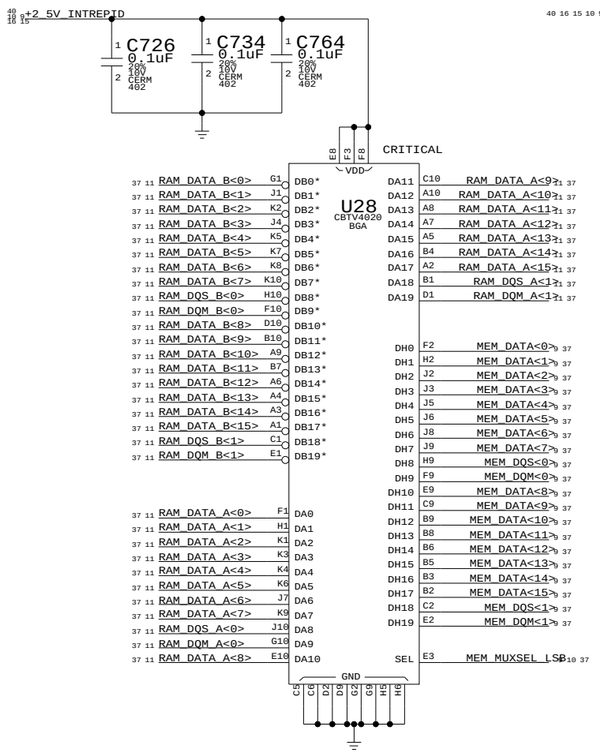
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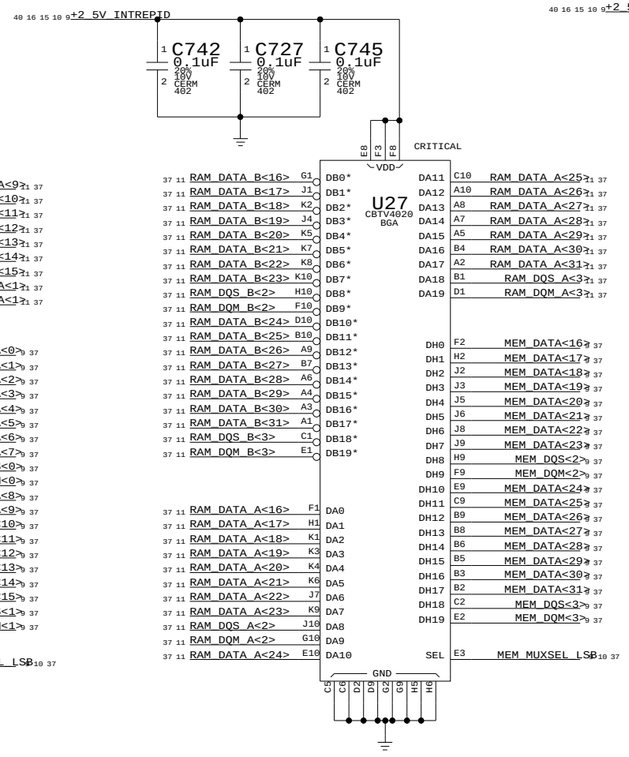
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D	051-6680	A
SCALE: NONE	SHT 9 OF 46	

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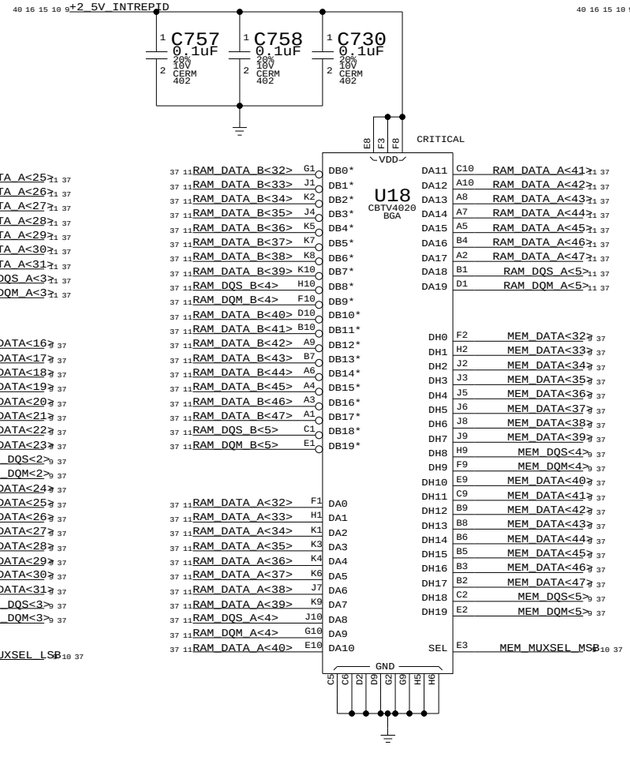
BIT 0..15



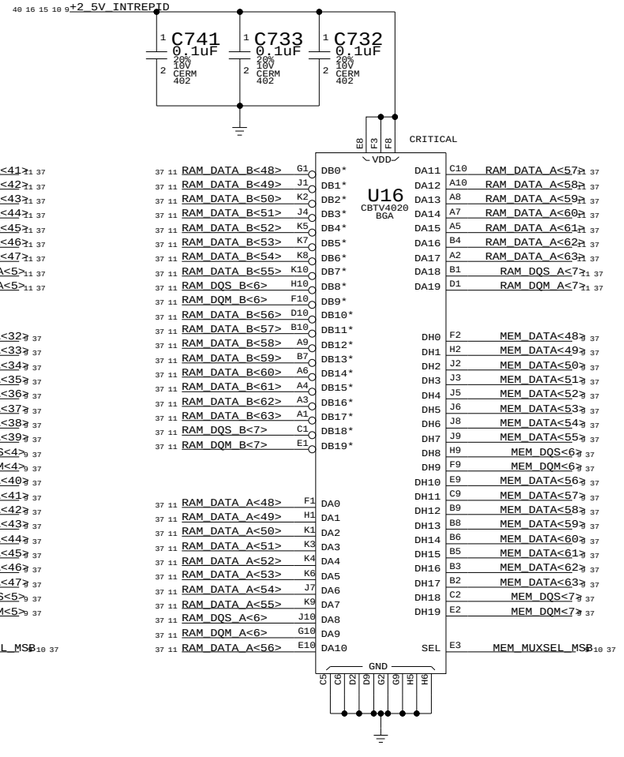
BIT 16..31



BIT 32..47



BIT 48..63



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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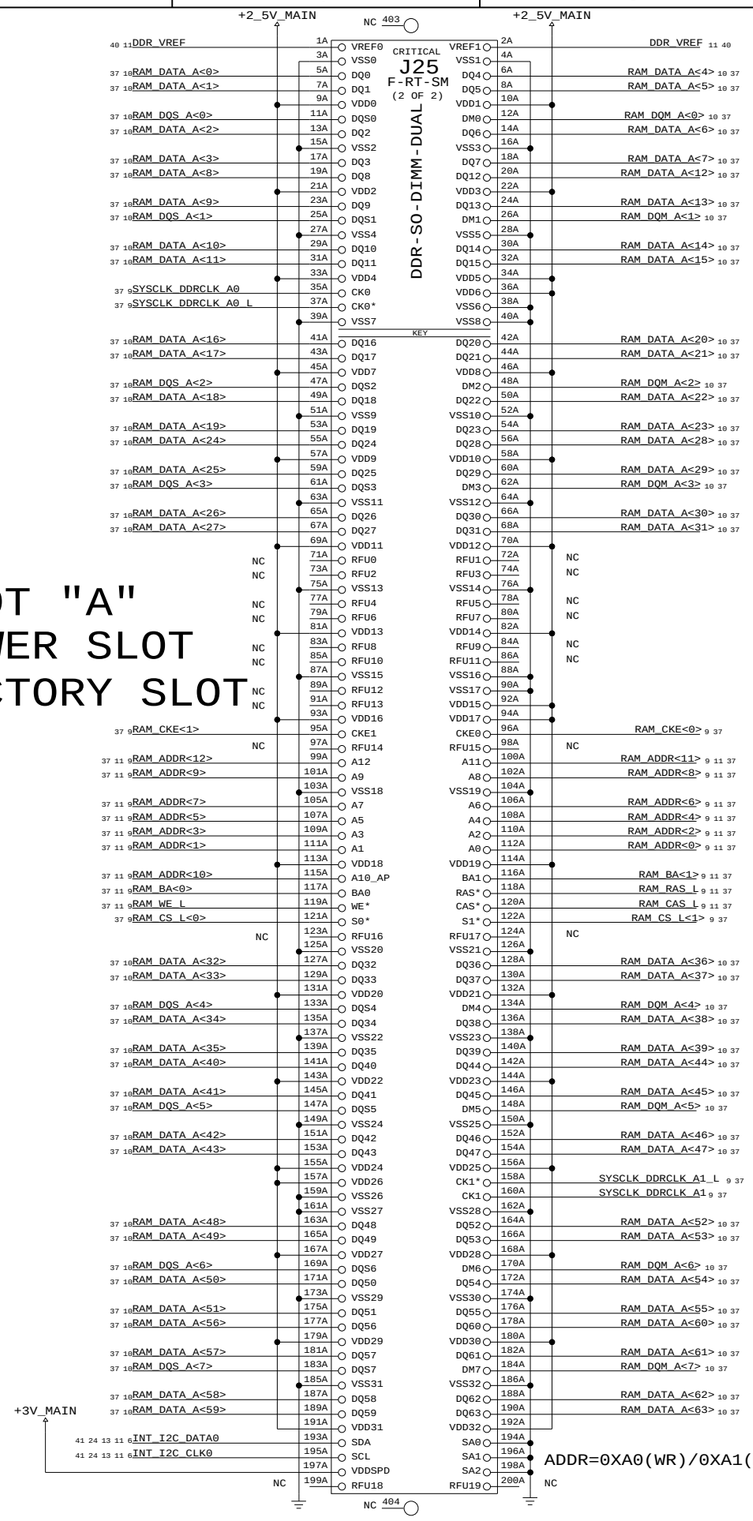
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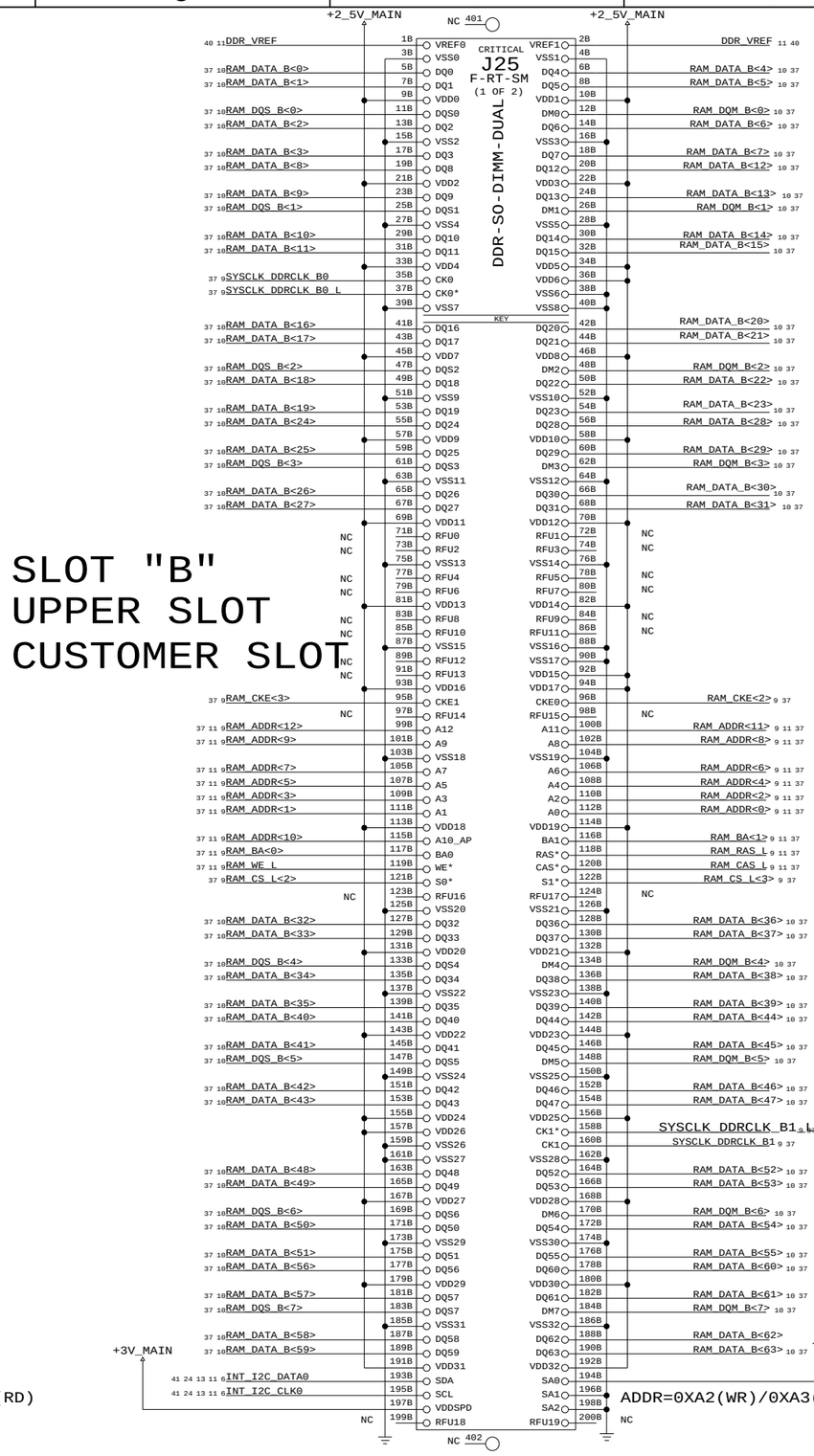
SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT OF
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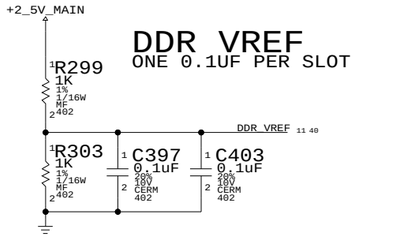


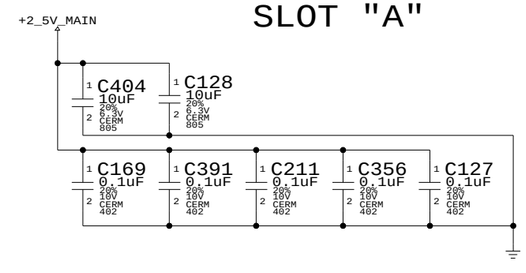
SLOT "A"
LOWER SLOT
FACTORY SLOT

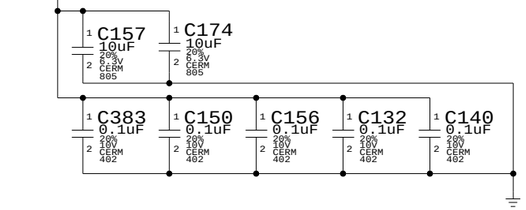


SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting







DDR SODIMM CONNS

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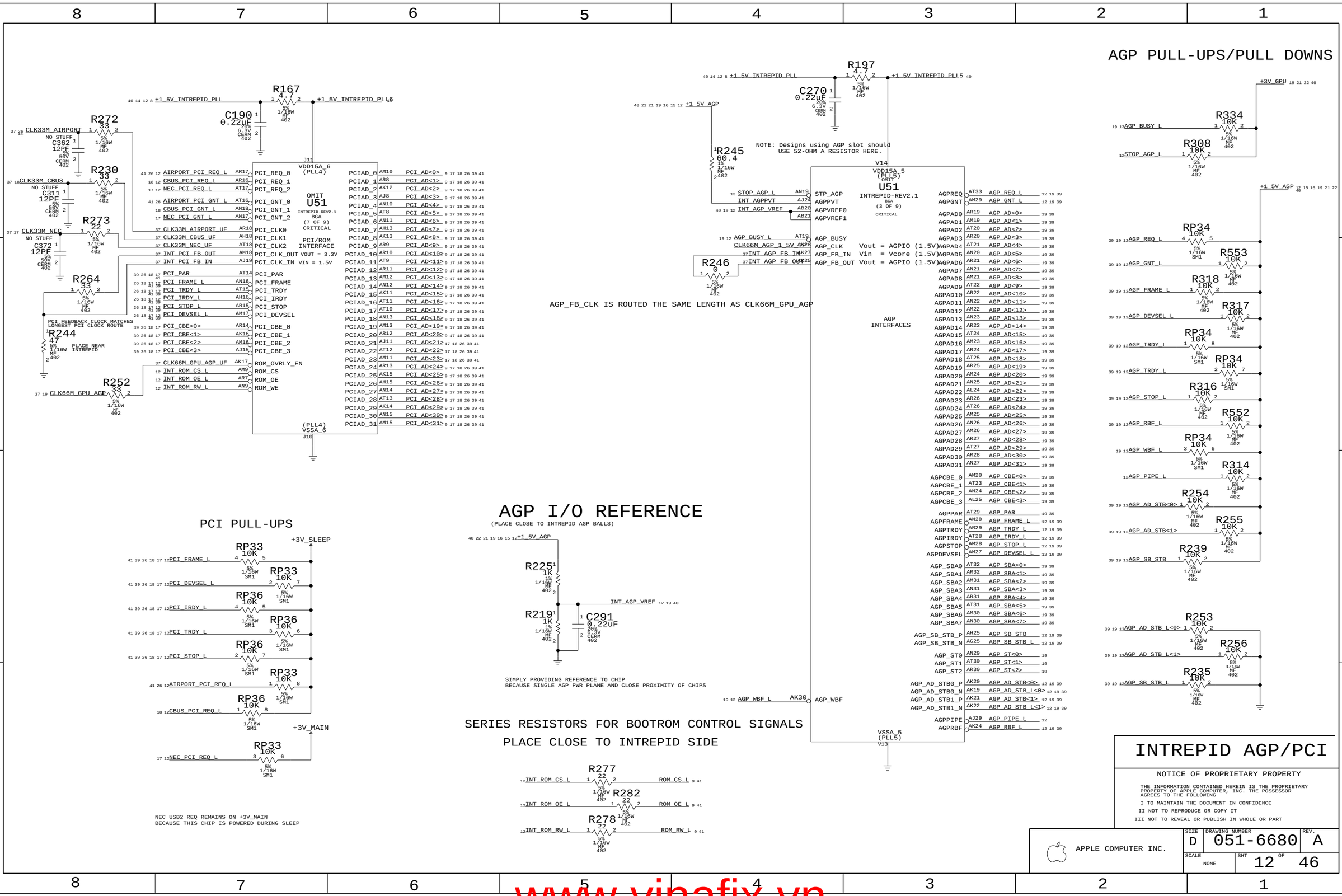
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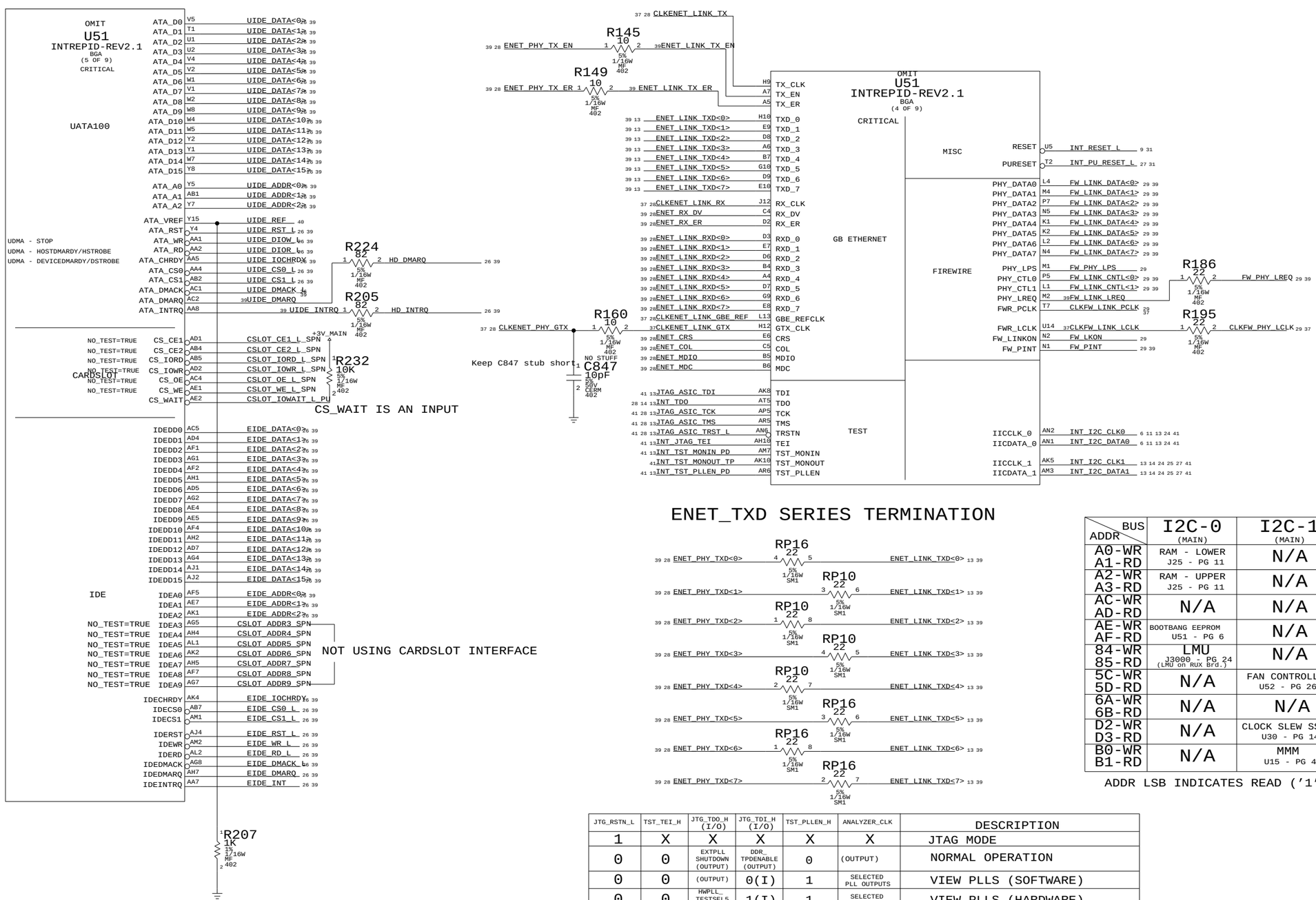
SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT OF
NONE	11 46

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USB PORT ASSIGNMENTS

PORT A B C D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R123 10K — USB_DBP
R121 10K — USB_DBM
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP — BT_USB_DP
R179 22 — USB_DEM — BT_USB_DM
R178 15K — R175 15K

PORT F/TRACKPAD

R635 22 — USB_DFP — USB_TPAD_P
R603 22 — USB_DFM — USB_TPAD_N
R129 15K — R125 15K

+2_5V_MAIN — NO STUFF R568 0 — +1_8V_MAIN — R565 0

U49 LTC1962-ADJ MSOP
IN ← +2_5V_MAIN (LTC1962_INT_VIN)
NC, NC
ADJ ← LTC1962_INT_ADJ
BYP → LTC1962_INT_BYP
SHDN
OUT → +1_5V_INTREPID_PLL (-> 1.55V OUTPUT)
C721 1uF 10V CERM 603
C392 0.01uF 20% 16V CERM 402
R574 18.7K 1% 1/16W MF 402
R567 68.1K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805

+3V_SLEEP
R148 10K — CBUS_INT_L
R746 10K — AIRPORT_PCI_INT_L
+3V_MAIN
R158 10K — NEC_PCI_INT_L
PCI INTERRUPTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

+3V_MAIN
GPIO/EXTINT PULLUPS
R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP6 10K — INT_EXTINT10_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K — INT_MOD_DTO_UF
RP15 10K — INT_MOD_CLKOUT_UF
RP5 10K — NC EXTINT11
RP4 10K — NC EXTINT12
RP15 10K — INT_MOD_DTI
RP15 10K — INT_MOD_SYNC_UF
R206 10K — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

+3V_MAIN — SSCG L15 400-OHM-EMI SM-1
+2_5V_MAIN — SSCG L14 400-OHM-EMI SM-1
+3V_CG_PLL_MAIN
MAIN_RESET_L
NO STUFF R286 0
SSCG R287 10K
SSCG C400 0.1uF
SSCG C402 1uF
SSCG C399 0.1uF
+2_5V_CG_MAIN
SSCG C394 0.1uF
SSCG R288 10K
NO STUFF R295 10K

U31 CY28512D TSSOP OMIT — CRITICAL
CLKIN 20 ← 37 14 INT_REF_CLK_OUT
FSEL 3 ← 14 CG_FSEL — INTERNAL 250K PULL-UP
SCLK 9 ← 14 INT_I2C_CLK1
SDATA 8 ← 14 INT_I2C_DATA1
ADDRSEL 14 ← CG_ADDRSEL — INTERNAL 250K PULL-DOWN
RESET* 17 ← CG_RESET_L
PD* 13 ← CG_SYSCLK_EN
LOCK 2 → CG_LOCK — OPEN DRAIN OUTPUT
ODSEL 4 ← NC — INTERNAL 250K PULL-UP
CPU0 16 → CG_CLKOUT
VDD0 1, VDD1 10, VDDA 12, VDDC 5, VDD0 18
VSS0 7, VSS1 19, VSSA 11, VSSC 6, VSSQ 15
OUTPUT IMPEDANCE ~18-20 OHMS

SSCG R293 33 — INT_REF_CLK_IN
SSCG R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
SSCG R284 0 — VCORE_VGATE
NO STUFF R296 10K
SSCG R142 0 — VCORE_VGATE

NO STUFF R467 0 — SYSTEM_CLK_EN
R457 0 — INT_TDO — CG_SYSCLK_EN
NO STUFF J9 U.FL-R-SMT — CLK18M_INT_EXT
NO STUFF R134 0
NO STUFF R113 51
NO STUFF R144 10M
R143 0
CRITICAL Y2 OMIT 18.432M 8X4.5MM-SM
C152 22pF — C151 22pF
CLK18M_XTAL_IN
R218 0 — INT_REF_CLK_OUT
CRYSTAL LOAD CAPACITANCE IS 16PF

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y2	CRITICAL	?

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

R240 4.7 — +1_5V_INTREPID_PLL
C337 0.22uF — R280 4.7 — +1_5V_INTREPID_PLL
C389 0.22uF — R279 4.7 — +1_5V_INTREPID_PLL
C388 0.22uF — R243 4.7 — +1_5V_INTREPID_PLL
C386 0.22uF — R201 4.7 — +1_5V_INTREPID_PLL
C387 0.22uF

+3V_MAIN — L13 FERR-EMI-100-OHM SM
+3V_INTREPID_USB
C235 0.01uF — C246 0.1uF — C256 10uF

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9) — OMIT

PCI VDD15A_1 (PLL1) AA16
PCI VDD15A_2 (PLL2) AJ12
PCI VDD15A_3 (PLL3) AJ17
PCI VDD15A_4 (PLL7) AJ18
PCI VDD15A_8 (PLL9) AG29
VDDU33_1 T8
VDDU33_2 U8

GPIO0 — VCORE A/B SEL
GPIO1 — GENERAL PURPOSE I/O'S
GPIO2 ... GPIO16
CG_FSEL_1 → CG_FSEL_INT (G5)
INT_GPIO1_PU (E1)
NC J7
COMM_RESET_L (F2)
FW_PHY_PD (J8)
SND_HP_MUTE_L (H5)
SND_AMP_MUTE_L (L9)
INT_GPIO9_PU (H4)
SND_HW_RESET_L (J5)
INT_GPIO12_PU (K8)
INT_GPIO15_PU (F1)
INT_ENET_RST_L (K7)

EXTINT0 ... EXTINT17 — INTERRUPTS
COMM_RING_DET_L (F33)
PMU_INT_L (E34)
AGP_ATI_INT_L (C33)
INT_EXTINT3_PU (D34)
SND_LIN_SENSE_L (B33)
ENET_ENERGY_DET (A33)
AIRPORT_PCI_INT_L (E31)
CBUS_INT_L (G36)
INT_EXTINT8_PU (D31)
PMU_INT_NMI (C32)
INT_EXTINT10_PU (B32)
MMM_FFIRQ_L (E30)
MMM_SIRQ_L (J9)
INT_EXTINT13_PU (F4)
INT_EXTINT14_PU (D1)
SND_HP_SENSE_L (E2)
INT_EXTINT16_PU (H7)
NEC_PCI_INT_L (G4)
MPIC_CPU_INT_L (D36)
PMU_PME_L (AJ7)
INT_PROC_SLEEP_REQ_L (AT6)
INT_PEND_PROC_INT (AN8)
CPU_INT

PCIPME
PROCSLEEPREQ
PENDPROCINT

XTAL_IN (U4)
XTAL_OUT (V1)
STOPXTAL — CLOCKS
SYSTEM_CLK_EN (AN7)
WATCHDOG
INT_WATCHDOG_L (AT7)
BUF_REF_CLK_OUT
SS_REF_CLK_IN
INT_REF_CLK_OUT_UF (U15)
INT_REF_CLK_IN (K9)

IICCLK_2 (AL4)
IICDATA_2 (AH8) — IIC

VSSA1 (PLL1) AA15
VSSA2 (PLL2) AJ13
VSSA3 (PLL3) AJ16
VSSA4 (PLL7) AK18
VSSA_8 (PLL9) AH29
VSSU_1 R9
VSSU_2 R8

SCCTXDA AF9 COMM_TXD_L (27 41)
SCCRTSA AN3 COMM_RTS_L (27 41)
SCCDTRA AF10 COMM_DTR_L (27 41)
SCCRXDA AG11 COMM_RXD (27 41)
SCCGPIOA AG9 COMM_GPIO_L (27 41)
VIA SCCTRXCA AT4 COMM_TRXC (27 41)
MISO SCCTXDB AR4 PMU_FROM_INT (31)
REQ* SCCRTSB AL5 PMU_REQ_L (14 31)
MOSI SCCRXDB AG10 PMU_TO_INT (31)
ACK* SCCGPIOB AP4 PMU_ACK_L (31)
SCK SCCTRXCB AM5 PMU_CLK (31)

USB
USB_VD0_P L8 USB_DAP (14)
USB_VD0_N L7 USB_DAM (14)
USB_VD1_P G2 USB_DBP (14)
USB_VD1_N G1 USB_DBM (14)
USB_PRTPWR0 J4 USB_PWREN_AB_L (14)
USB_PWRFLT0 K4 USB_OC_AB_L (14)
USB_VD2_P H2 USB_DCP (14)
USB_VD2_N H1 USB_DCM (14)
USB_VD3_P M7 USB_DDP (14)
USB_VD3_N M8 USB_DDM (14)
USB_PRTPWR1 J2 USB_PWREN_CD_L (14)
USB_PWRFLT1 J1 USB_OC_CD_L (14)
USB_VD4_P K5 USB_DEP (14 39)
USB_VD4_N L5 USB_DEM (14 39)
USB_VD5_P P8 USB_DFP (14 39)
USB_VD5_N N8 USB_DFM (14 39)
USB_PRTPWR2 M5 USB_PWREN_EF_L (14)
USB_PWRFLT2 N7 USB_OC_EF_L (14)

AUDIO/I2S
AUD_DTO R4 INT_I2S0_SND_TO_DAC_UF (41)
AUD_DTI R7 INT_I2S0_SND_FROM_ADC_UF (41)
AUD_SYNC T5 INT_I2S0_SND_LRCLK_UF
AUD_BITCLK P2 INT_I2S0_SND_SCLK_UF
AUD_CLKOUT R5 INT_I2S0_SND_MCLK_UF
MOD_DTO R2 INT_MOD_DTO_UF (14)
(SIGNAL FROM MODEM) MOD_DTI T4 INT_MOD_DTI (14 27)
MOD_SYNC R1 INT_MOD_SYNC_UF (14)
MOD_BITCLK V8 INT_MOD_BITCLK_UF (14)
MOD_CLKOUT P1 INT_MOD_CLKOUT_UF (14)

RP13 47 — INT_I2S0_SND_TO_DAC (41)
RP13 47 — INT_I2S0_SND_LRCLK (41)
RP13 47 — INT_I2S0_SND_SCLK (41)
RP13 47 — INT_I2S0_SND_MCLK (37 41)
SOFT_MODEM RP47 0K — INT_MOD_DTO (7)
SOFT_MODEM RP47 0K — INT_MOD_SYNC (7)
SOFT_MODEM RP47 0K — INT_MOD_BITCLK (7)
SOFT_MODEM RP47 0K — INT_MOD_CLKOUT (7)

+3V_SLEEP
2R258 1K — INT_I2C_CLK (2 41)
2R241 1K — INT_I2C_DATA (2 41)

INT - USB/GPIOS/I2S

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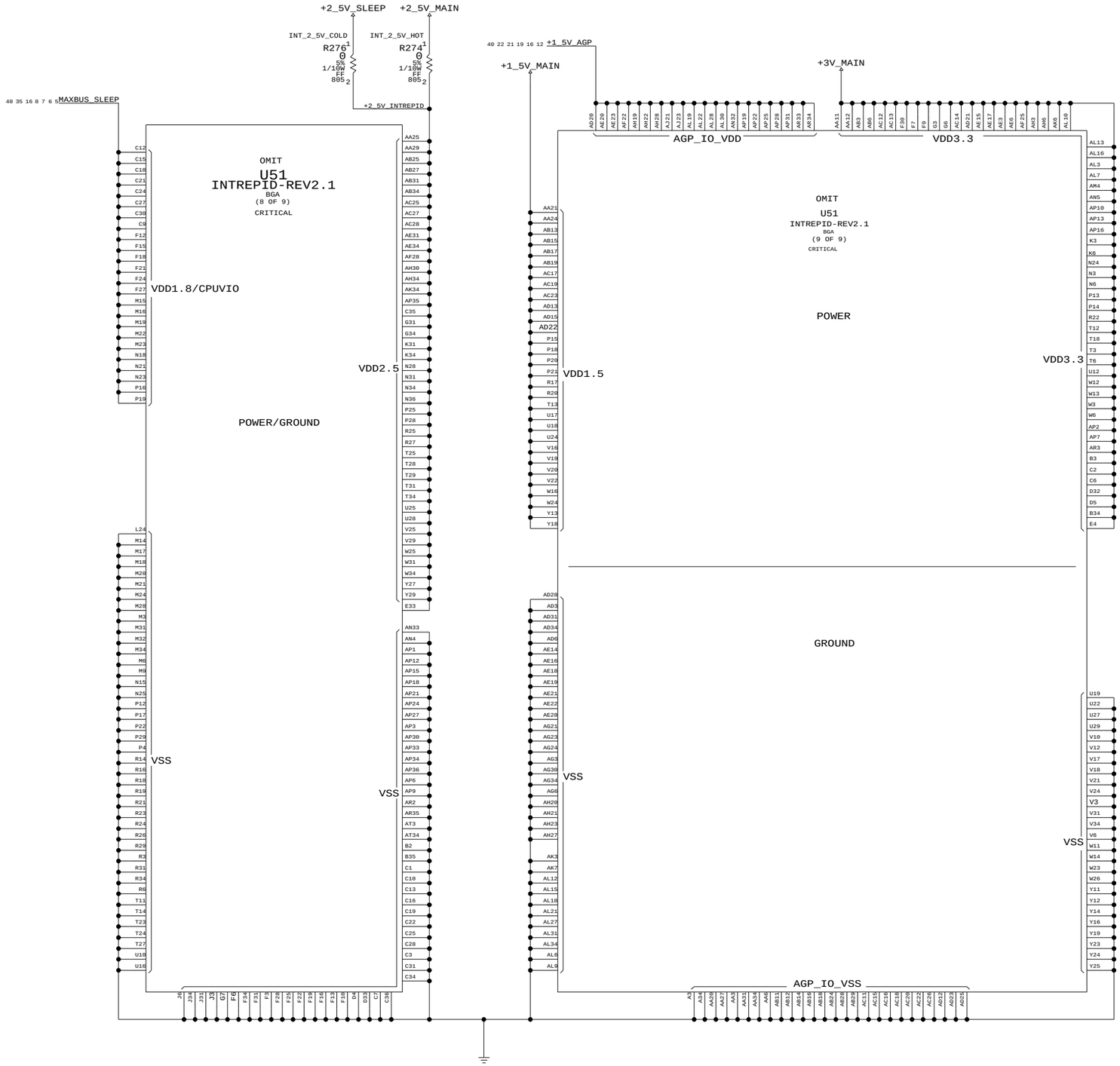
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 14 OF 46	

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT
NONE	15 OF 46

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INTREPID MAXBUS DECOUPLING

35 15 8 7 6 5 MAXBUS_SLEEP 40

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

C148 10uF 20% 6.3V CERM 805 · C142 10uF 20% 6.3V CERM 805 · C144 10uF 20% 6.3V CERM 805 · C146 10uF 20% 6.3V CERM 805

C182 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C164 0.22uF 20% 6.3V CERM 402 · C225 0.22uF 20% 6.3V CERM 402 · C160 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402

C204 0.22uF 20% 6.3V CERM 402 · C166 0.22uF 20% 6.3V CERM 402 · C205 0.22uF 20% 6.3V CERM 402 · C223 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C183 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402

C165 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C147 0.22uF 20% 6.3V CERM 402 · C149 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C324 10uF 20% 6.3V CERM 805 · C325 10uF 20% 6.3V CERM 805 · C201 10uF 20% 6.3V CERM 805 · C200 10uF 20% 6.3V CERM 805

C299 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C302 0.22uF 20% 6.3V CERM 402 · C300 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C272 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402

C301 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C224 0.22uF 20% 6.3V CERM 402 · C222 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402

C271 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C303 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C258 0.22uF 20% 6.3V CERM 402 · C236 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

40 22 21 19 15 12 +1_5V_AGP

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

C381 10uF 20% 6.3V CERM 805 · C380 10uF 20% 6.3V CERM 805 · C382 10uF 20% 6.3V CERM 805 · C379 10uF 20% 6.3V CERM 805

C367 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C330 0.22uF 20% 6.3V CERM 402 · C363 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402 · C332 0.22uF 20% 6.3V CERM 402 · C361 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C328 0.22uF 20% 6.3V CERM 402 · C364 0.22uF 20% 6.3V CERM 402

C365 0.22uF 20% 6.3V CERM 402 · C329 0.22uF 20% 6.3V CERM 402 · C345 0.22uF 20% 6.3V CERM 402 · C346 0.22uF 20% 6.3V CERM 402 · C373 0.22uF 20% 6.3V CERM 402 · C344 0.22uF 20% 6.3V CERM 402 · C331 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C347 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

C378 10uF 20% 6.3V CERM 805 · C376 10uF 20% 6.3V CERM 805 · C377 10uF 20% 6.3V CERM 805 · C375 10uF 20% 6.3V CERM 805

C170 0.22uF 20% 6.3V CERM 402 · C358 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C327 0.22uF 20% 6.3V CERM 402 · C342 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402

C175 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C189 0.22uF 20% 6.3V CERM 402 · C167 0.22uF 20% 6.3V CERM 402 · C371 0.22uF 20% 6.3V CERM 402 · C359 0.22uF 20% 6.3V CERM 402

C285 0.22uF 20% 6.3V CERM 402 · C283 0.22uF 20% 6.3V CERM 402 · C269 0.22uF 20% 6.3V CERM 402 · C221 0.22uF 20% 6.3V CERM 402 · C234 0.22uF 20% 6.3V CERM 402 · C247 0.22uF 20% 6.3V CERM 402 · C257 0.22uF 20% 6.3V CERM 402 · C343 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C228 0.22uF 20% 6.3V CERM 402

C360 0.22uF 20% 6.3V CERM 402 · C308 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C341 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

40 15 10 9 +2_5V_INTREPID

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

C314 10uF 20% 6.3V CERM 805 · C322 10uF 20% 6.3V CERM 805 · C191 10uF 20% 6.3V CERM 805 · C202 10uF 20% 6.3V CERM 805

C304 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C281 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C253 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C348 0.22uF 20% 6.3V CERM 402 · C192 0.22uF 20% 6.3V CERM 402

C306 0.22uF 20% 6.3V CERM 402 · C252 0.22uF 20% 6.3V CERM 402 · C275 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C218 0.22uF 20% 6.3V CERM 402 · C274 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C168 0.22uF 20% 6.3V CERM 402

C265 0.22uF 20% 6.3V CERM 402 · C251 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402 · C254 0.22uF 20% 6.3V CERM 402 · C305 0.22uF 20% 6.3V CERM 402 · C186 0.22uF 20% 6.3V CERM 402 · C219 0.22uF 20% 6.3V CERM 402 · C315 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402

C323 0.22uF 20% 6.3V CERM 402 · C273 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C203 0.22uF 20% 6.3V CERM 402 · C333 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C231 0.22uF 20% 6.3V CERM 402 · C296 0.22uF 20% 6.3V CERM 402

C239 0.22uF 20% 6.3V CERM 402 · C316 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C282 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402

INTREPID/MAIN 2.5V DECOUPLING

+2_5V_MAIN

10 X 0.22UF (0402)

C770 0.22uF 20% 6.3V CERM 402 · C139 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C735 0.22uF 20% 6.3V CERM 402 · C245 0.22uF 20% 6.3V CERM 402 · C736 0.22uF 20% 6.3V CERM 402 · C739 0.22uF 20% 6.3V CERM 402 · C395 0.22uF 20% 6.3V CERM 402 · C374 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE		SHT 16 OF 46

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

+3V_NEC_VDD 17 40

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

40 NEC_AVDD

40 17 +3V_NEC_VDD

Y1's LOAD CAPACITANCE = 16 pF

OMIT CRITICAL
Y1 30.0000M
8X4.5MM-SM

NEC_XT2_R

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

R613 43.2 1% 1/16W MF 402 — NEC_USB_DAM 27 39 41
R612 43.2 1% 1/16W MF 402 — NEC_USB_DAP 27 39 41
R609 43.2 1% 1/16W MF 402 — NEC_USB_DBM 27 39 41
R610 43.2 1% 1/16W MF 402 — NEC_USB_DBP 27 39 41

Low/Full/High Speed (External)
Low/Full/High Speed (External)

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 M12 — AVDD
VDD_PCI

41 39 26 18 12 9 PCI_AD<0>	M5	AD0
41 39 26 18 12 9 PCI_AD<1>	P5	AD1
41 39 26 18 12 9 PCI_AD<2>	N5	AD2
41 39 26 18 12 9 PCI_AD<3>	P4	AD3
41 39 26 18 12 9 PCI_AD<4>	N4	AD4
41 39 26 18 12 9 PCI_AD<5>	M3	AD5
41 39 26 18 12 9 PCI_AD<6>	N3	AD6
41 39 26 18 12 9 PCI_AD<7>	M1	AD7
41 39 26 18 12 9 PCI_AD<8>	L2	AD8
41 39 26 18 12 9 PCI_AD<9>	L1	AD9
41 39 26 18 12 9 PCI_AD<10>	K2	AD10
41 39 26 18 12 9 PCI_AD<11>	L3	AD11
41 39 26 18 12 9 PCI_AD<12>	K1	AD12
41 39 26 18 12 9 PCI_AD<13>	K3	AD13
41 39 26 18 12 9 PCI_AD<14>	J2	AD14
41 39 26 18 12 9 PCI_AD<15>	J1	AD15
41 39 26 18 12 9 PCI_AD<16>	F2	AD16
41 39 26 18 12 9 PCI_AD<17>	E3	AD17
41 39 26 18 12 9 PCI_AD<18>	E1	AD18
41 39 26 18 12 9 PCI_AD<19>	D3	AD19
41 39 26 18 12 9 PCI_AD<20>	D1	AD20
41 39 26 18 12 PCI_AD<21>	D2	AD21
41 39 26 18 12 PCI_AD<22>	C2	AD22
41 39 26 18 12 PCI_AD<23>	C1	AD23
41 39 26 18 12 9 PCI_AD<24>	B4	AD24
41 39 26 18 12 9 PCI_AD<25>	A4	AD25
41 39 26 18 12 9 PCI_AD<26>	B5	AD26
(PCI_AD<27>)	C4	AD27
41 39 26 18 12 9 PCI_AD<28>	A5	AD28
41 39 26 18 12 9 PCI_AD<29>	C5	AD29
41 39 26 18 12 9 PCI_AD<30>	B6	AD30
41 39 26 18 12 9 PCI_AD<31>	A6	AD31
39 26 18 12 PCI_CBE<0>	M2	CBE0
39 26 18 12 PCI_CBE<1>	J3	CBE1
39 26 18 12 PCI_CBE<2>	F1	CBE2
39 26 18 12 PCI_CBE<3>	C3	CBE3
41 39 26 18 12 PCI_PAR	J4	PAR
41 39 26 18 12 PCI_FRAME_L	F3	FRAME
41 39 26 18 12 PCI_IRDY_L	F4	IRDY
41 39 26 18 12 PCI_TRDY_L	G1	TRDY
41 39 26 18 12 PCI_STOP_L	G3	STOP
NEC_IDSEL	B3	IDSEL
41 39 26 18 12 PCI_DEVSEL_L	G2	DEVSEL
12 NEC_PCI_REQ_L	C6	REQ
12 NEC_PCI_GNT_L	D6	GNT
18 PCI_PERR_L	H2	PERR
18 PCI_SERR_L	H1	SERR
NEC_PCI_INTA_L	C7	INTA
NEC_PCI_INTB_L	B7	INTB
NEC_PCI_INTC_L	A7	INTC
37 12 CLK33M_NEC	A8	PCLK
17 NEC_IO_RESET_L	B8	VBRRST
NEC_CRUN_L	N6	CRUN
17 NEC_PME_L	D8	PME
17 NEC_MAIN_RESET_L	C8	VCCRST
NEC_SMI_L_TP	L6	SMI
17 NEC_LEGC	L7	LEGC

R636 22 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP45 47 5% 1/16W SM1
NC — NEC_PCI_INT

R617 4.7k 5% 1/16W MF 402

RP44 47 5% 1/16W SM1

31 28 25 24 IO_RESET_L	1	8 NEC_IO_RESET_L 17
41 31 26 14 PMU_PME_L	2	7 NEC_PME_L 17
41 31 26 20 19 18 14 MAIN_RESET_L	3	6 NEC_MAIN_RESET_L 17
17 NEC_LEGC	4	5

VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK	L9	NEC_XT1
XT2	P8	NEC_XT2
RSDM1	M14	NEC_USB_RSDM1
DM1	M13	(NEC_USB_DAM)
DP1	L14	(NEC_USB_DAP)
RSDP1	K13	NEC_USB_RSDP1
RSDM2	K14	NEC_USB_RSDM2
DM2	K12	(NEC_USB_DBM)
DP2	J14	(NEC_USB_DBP)
RSDP2	J12	NEC_USB_RSDP2
RSDM3	H11	NC
DM3	G11	
DP3	G13	
RSDP3	G14	NC
RSDM4	F12	NC
DM4	F14	
DP4	E12	
RSDP4	E14	NC
RSDM5	E13	NC
DM5	D14	
DP5	C13	
RSDP5	C14	NC
RREF	P11	NEC_RREF

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F 17

OCI1	B12	NEC_LUSB_OCI
OCI2	B11	NEC_RUSB_OCI
OCI3	B10	NEC_OCI<3>
OCI4	A10	NEC_OCI<4>
OCI5	B9	NEC_OCI<5>
PPON1	C12 OUT	NEC_LUSB_PPON 41
PPON2	A11 OUT	NEC_RUSB_PPON 41
PPON3	C11 OUT	NEC_PPON3_TP
PPON4	C10 OUT	NEC_PPON4_TP
PPON5	A9 OUT	NEC_PPON5_TP
NC1	P6	NEC_NC<1>
NC2	M6	NEC_NC<2>

RP43 10K 5% 1/16W SM1 — +3V_NEC_VDD 17 40
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

NEC documentation indicates that NCs must be tied high.

NTEST1	M8 IPD	NC
SMC	M7 IPD	NC
TEB	N7 IPD	NC
AMC	P7 IPD	NEC_AMC_TP
TEST	L8 IPD	NC
NANDTEST	M10	NEC_NANDTESTEN_TP
SRCLK	M9	NC
SRDTA	N9	NEC_NANDTESTOUT_TP
SRMOD	P9 IPD	NC
AVSS	N11 P13 M12	AVSS(R)

R798 0 5% 1/16W MF 603 — NEC_AVSS_F

+3V_MAIN

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1

R607 0 5% 1/16W MF 402 — 17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 27 41
R608 0 5% 1/16W MF 402 — 17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 27 41

NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

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PCI1510 PULL-UPS

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

INTEGRATED PULL-UP

PC CARD/CARDBUS CONNECTOR

J5 QT500806-L111 M-ST-SM1

U8 PCI1510GGU BGA

U4 TPS2211

CRITICAL CLAMP FOR PC-CARD CLAMP FOR PCI

CARDBUS

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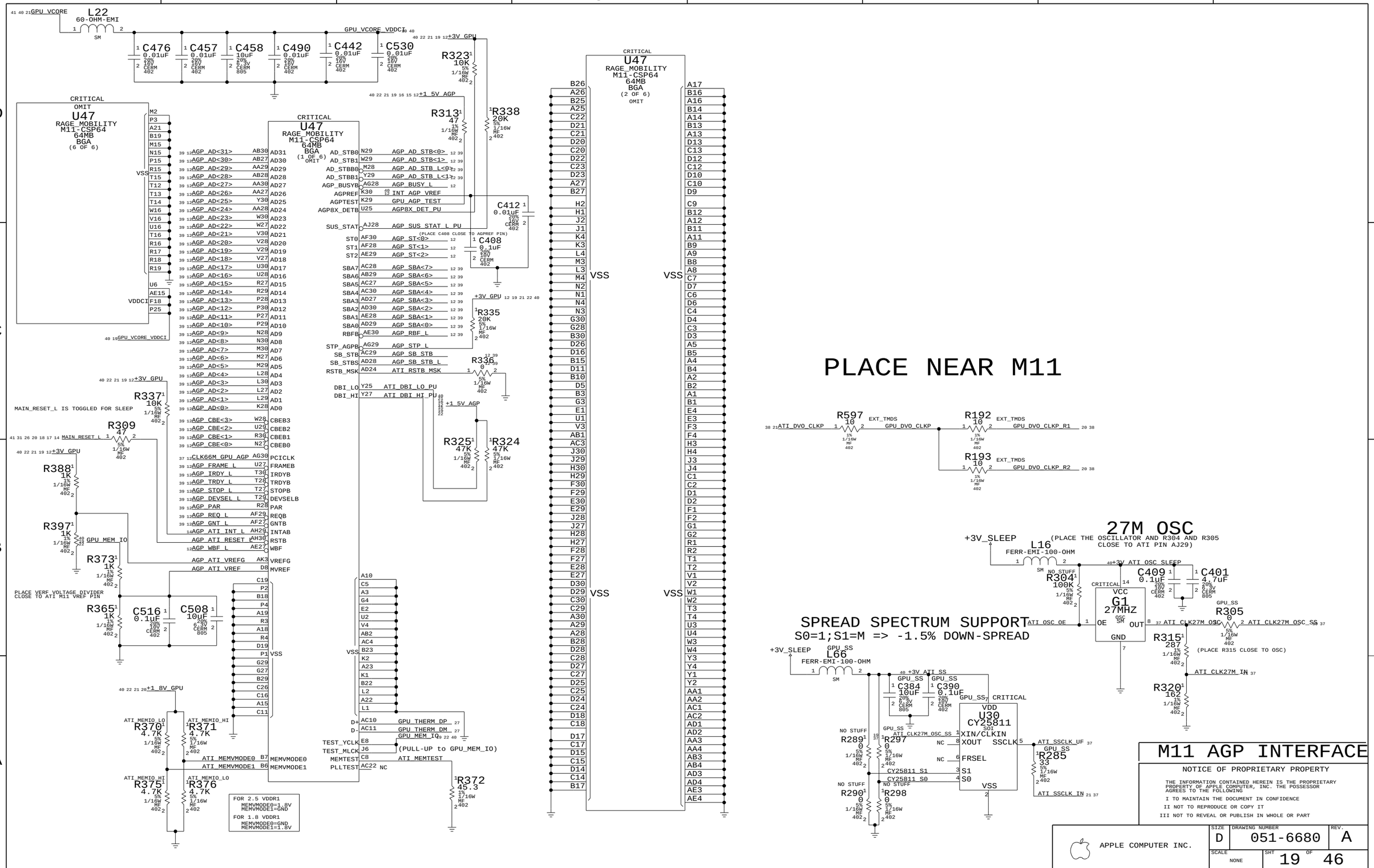
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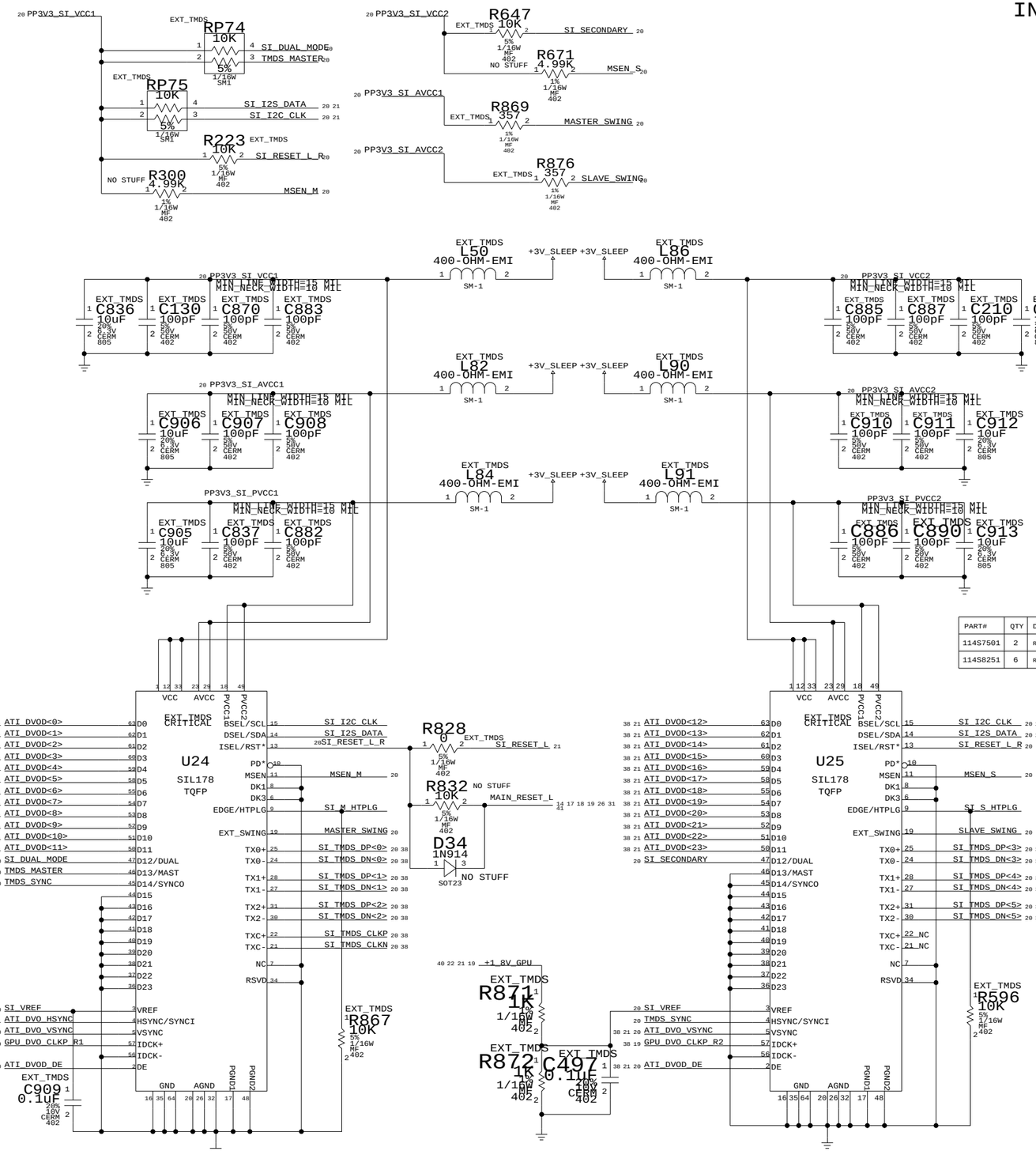
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S7501	2	RES, MF, 1/16W, 75 OHM, 1%, 0402, SMD	R374, R377		EXT_TMDS
114S8251	6	RES, MF, 1/16W, 82.5 OHM, 1%, 0402, SMD	R340, R350, R355, R362, R367, R369		EXT_TMDS

INT/EXT TMDS

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GPU VCORE - 1.2V

(PUT ALL CAPS BELOW ATI ASIC)

GPU VCORE SUPPLY

M10 Power Shut down Sequencing

PLACE ALL TMDS 0 OHMS close to GPU

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

M11 CORE PWR/LVDS/TMDS

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GPU PLL - 1.8V

+2_5V_SLEEP
U34 MM1571J SOT-25A (150mA MAX) CRITICAL
VIN VOUT CONT NOISE GND
GPU_CORE_OK
ATI_PVDD_BYP
C830 1uF 20% 10V CERM 603
C553 0.01uF 20% 10V CERM 402
1_8V_PVDD_STD
R787 0 5% 1/16W MF 402
+1_8V_ATI_PVDD
L20 FERR-220-OHM 0402
+1_8V_GPU_PLL
C418 10uF 20% 6.3V CERM 805
C414 0.1uF 20% 10V CERM 402
C413 0.01uF 20% 10V CERM 402 (21mA)
C552 10uF 20% 6.3V CERM 805
+1_8V_GPU
L19 FERR-220-OHM 0402
+1_8V_GPU_AVDD (AVDD+VDDDI=75mA)
C427 10uF 20% 6.3V CERM 805
C453 0.01uF 20% 10V CERM 402
C450 0.01uF 20% 10V CERM 402

+2_5V_SLEEP
L23 FERR-220-OHM 0402 (140mA) +2_5V_GPU_A2VDD
C459 10uF 20% 6.3V CERM 805
C460 0.01uF 20% 10V CERM 402
C461 0.01uF 20% 10V CERM 402

+1_8V_GPU
L21 FERR-220-OHM 0402 (2mA) +1_8V_GPU_AVDDQ
C464 10uF 20% 6.3V CERM 805
C463 0.01uF 20% 10V CERM 402

+1_8V_GPU
L24 FERR-220-OHM 0402 (AVDD+VDDDI=75mA) +1_8V_GPU_VDDDI
C478 10uF 20% 6.3V CERM 805
C462 0.01uF 20% 10V CERM 402
C454 0.01uF 20% 10V CERM 402

+2_5V_SLEEP
L28 FERR-220-OHM 0402 +2_5V_GPU_MCLK
C511 10uF 20% 6.3V CERM 805
C527 0.01uF 20% 10V CERM 402
C472 0.01uF 20% 10V CERM 402

+1_5V_SLEEP
R275 0 5% 1/10W FF 805
+1_5V_AGP
1.5V

+1_8V_SLEEP
R363 0 5% 1/10W FF 805
+1_8V_GPU
1.8V

+1_8V_SLEEP +2_5V_SLEEP
ATI_MEMIO_LO R312 0 5% 1/10W FF 805
ATI_MEMIO_HI R319 0 5% 1/10W FF 805
GPU_MEM_IO
1.8V 2.5V

+3V_SLEEP
R379 0 5% 1/10W FF 805
+3V_GPU
3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

AGP 4X I/O - 1.5V

+1_5V_AGP
L18 FERR-10-OHM-500MA SM (20mA)
C438 0.1uF 20% 10V CERM 402
C444 0.1uF 20% 10V CERM 402
C423 0.1uF 20% 10V CERM 402
C424 0.1uF 20% 10V CERM 402
C422 10uF 20% 6.3V CERM 805
C439 0.01uF 20% 10V CERM 402
C447 0.01uF 20% 10V CERM 402
C425 0.01uF 20% 10V CERM 402
C417 0.01uF 20% 10V CERM 402

MEMORY CORE - 2.5V

+2_5V_SLEEP
L25 FERR-220-OHM 0805 (1800mA)
+2_5V_GPU_MEMCORE
C470 0.1uF 20% 10V CERM 402
C539 0.1uF 20% 10V CERM 402
C475 0.1uF 20% 10V CERM 402
C419 0.1uF 20% 10V CERM 402
C483 10uF 20% 6.3V CERM 805
C471 0.01uF 20% 10V CERM 402
C538 0.01uF 20% 10V CERM 402
C504 0.01uF 20% 10V CERM 402
C420 0.01uF 20% 10V CERM 402

LVDS PLL - 1.8V

+1_8V_ATI_PVDD
L32 FERR-220-OHM 0402
+1_8V_GPU_PNLPLL (40mA)
C493 10uF 20% 6.3V CERM 805
C468 0.01uF 20% 10V CERM 402

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD
L30 FERR-220-OHM 0402
+1_8V_GPU_MEMPLL
C537 10uF 20% 6.3V CERM 805
C523 0.01uF 20% 10V CERM 402
+1_8V_GPU_TP_PLL
C831 10uF 20% 6.3V CERM 805
C832 0.01uF 20% 10V CERM 402

LVDS - 2.5V

+2_5V_SLEEP
L26 FERR-10-OHM-500MA SM (20mA)
+2_5V_GPU_PNLIO (350mA)
C499 10uF 20% 6.3V CERM 805
C500 0.01uF 20% 10V CERM 402
C473 0.01uF 20% 10V CERM 402

LVDS/TMDS - 1.8V

+1_8V_GPU
L29 FERR-220-OHM 0402
+1_8V_GPU_PNLIO (180mA)
C514 10uF 20% 6.3V CERM 805
C492 0.1uF 20% 10V CERM 402
C496 0.1uF 20% 10V CERM 402
C489 0.1uF 20% 10V CERM 402
C491 0.1uF 20% 10V CERM 402
C501 0.01uF 20% 10V CERM 402
C506 0.01uF 20% 10V CERM 402

AK29 PVDD
AF23 AVDD0
AF24 AVDD1
A2VDD0
A2VDD1
A2VDDQ
VDD1DI
VDD2DI
VDDRH0
VDDRH1
K25 L25 T25 Y28 K27 AA25 K26 L26 M26 N26 P26 R26 T26 U26 V26 Y26 AA26 AB26 AC26 VDDP
E5 E6 E12 E13 E18 E19 E20 E26 F26 VDDM
E7 H26 E9 E10 E11 E14 E15 E16 VDDR1 E17 E21 E22 E23 E24 E25
AK21 LPVDD
AK11 TPVDD
A7 MPVDD
AE16 AF16 LVDDR_18
AG16 AF17 LVDDR_25
AG12 TXVDDR0
AG13 TXVDDR1
AG14 TXVDDR2
AG15 TXVDDR3

PVSS AK30
AVSSQ AF22
A2VSSQ AJ22
AVSSN0 AE22
AVSSN1 AE23
A2VSSN0 AE19
A2VSSN1 AE20
VSS1DI AG23
VSS2DI AF19
VSSRH0 F20
VSSRH1 M6
F5 G5 H5 J5 K5 L5 M5 N5 P5 R5 T5 U5 V5 W5 Y5 AA5 AB5 AC5 AD5 G26 K6 R6 Y6 AA6 F8 F9 F15 F16 F21 F22 H25 J25 J26 VDDR1
AF6 AE7 AF7 AE8 VDDR4
AE9 AF9 AF10 AD25 AE25 AE26 AF26 VDDR3
AJ21 LPVSS
AJ11 TPVSS
A6 MPVSS
AH16 LVSSR0
AG17 LVSSR1
AH17 LVSSR2
AF18 LVSSR3
AH12 DVOVMODE
AH13 TXVSSR1
AH14 TXVSSR2
AH15 TXVSSR3

OMIT
CRITICAL
U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(4 OF 6)

+2_5V_GPU_A2VDD
+1_8V_GPU_AVDDQ
+1_8V_GPU_VDDDI
+2_5V_GPU_MCLK
GPU_MEM_IO

MEMORY I/O

+2_5V_SLEEP
U60 MM1571J SOT-25A (150mA MAX) CRITICAL
VIN VOUT CONT NOISE GND
GPU_CORE_OK
ATI_TPVDD_BYP
C833 1uF 20% 10V CERM 603
C834 0.01uF 20% 10V CERM 402
+1_8V_ATI_TPVDD
L75 FERR-220-OHM 0402
R788 0 5% 1/16W MF 402
1_8V_TPVDD_STD
C835 10uF 20% 6.3V CERM 805
GPU_MEM_IO
L31 FERR-220-OHM 0805
+1_8V_GPU (1200mA) GPU_MEM_IO_FLT
C551 10uF 20% 6.3V CERM 805
C421 0.1uF 20% 10V CERM 402
C456 0.1uF 20% 10V CERM 402
C488 0.1uF 20% 10V CERM 402
C517 0.1uF 20% 10V CERM 402
C546 0.1uF 20% 10V CERM 402
C545 0.1uF 20% 10V CERM 402
C544 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C541 0.1uF 20% 10V CERM 402
C436 0.1uF 20% 10V CERM 402
C437 0.1uF 20% 10V CERM 402
C540 0.1uF 20% 10V CERM 402
C547 0.1uF 20% 10V CERM 402
C542 0.01uF 20% 10V CERM 402

1.8V DVO POWER (EXT.TMDS)

+1_8V_GPU
EXT_TMDS L81 FERR-10-OHM-500MA SM
+1_8V_GPU_DVO
C535 10uF 20% 6.3V CERM 805
C519 0.1uF 20% 10V CERM 402
C534 0.1uF 20% 10V CERM 402
C521 0.1uF 20% 10V CERM 402
INT_TMDS R843 0 5% 1/16W MF 603

3.3V IO SUPPLY

(Max Current varies, depends on usage)

+3V_GPU
L33 FERR-10-OHM-500MA SM
+3V_GPU_FLT
C550 10uF 20% 6.3V CERM 805
C518 0.1uF 20% 10V CERM 402
C520 0.1uF 20% 10V CERM 402
C430 0.1uF 20% 10V CERM 402
C880 0.1uF 20% 10V CERM 402
C881 0.1uF 20% 10V CERM 402
C426 0.1uF 20% 10V CERM 402
+1_8V_GPU
EXT_TMDS R842 0 5% 1/16W MF 402
ATI_DVOVMODE
INT_TMDS R841 0 5% 1/10W MF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

M11 POWER

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EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
74AHC1G32 U40 (OMIT)
ATI_VSYNC → ATI_VSYNC_BUF → L38 FERR-60-OHM-0.1A (0402) → VGA_VSYNC
PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR
+3V_MAIN
74AHC1G32 U39 (OMIT)
ATI_HSYNC → ATI_HSYNC_BUF → L36 FERR-60-OHM-0.1A (0402) → VGA_HSYNC

TMDS FILTERING

PLACE CLOSE TO CONNECTOR

L37 370-OHM
TMDS_CLKP
TMDS_CLKN
TMDS CONN CLKP
TMDS CONN CLKN

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

FL1 LCFILTER SM-220MHZ CRITICAL — GPU_B → VGA_B
FL2 LCFILTER SM-220MHZ CRITICAL — GPU_G → VGA_G
FL3 LCFILTER SM-220MHZ CRITICAL — GPU_R → VGA_R

C641	3.3pF 0.25pF 50V CERM 402	R462 75 1% 1/16W MF 402 NO STUFF
C634	3.3pF 0.25pF 50V CERM 402	R458 75 1% 1/16W MF 402 NO STUFF
C631	3.3pF 0.25pF 50V CERM 402	R456 75 1% 1/16W MF 402 NO STUFF

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F2 0.5AMP-13.2V CRITICAL SM → +5V_DDC_SLEEP_UF → L42 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D19 MBR0530 SM: DDC_CLK_ISO

R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402

C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201
C667 0.01UF 10% 50V CERM 603

R464 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
R463 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19

J22 QHI112 F-RT-TH CRITICAL

CHGND1 / CHGND2

TMDS_DN<2>	TMDS_CONN_DN<2>	
TMDS_DP<2>	TMDS_CONN_DN<1>	
TMDS_DN<1>	TMDS_CONN_DP<2>	
TMDS_DP<1>	TMDS_CONN_DP<1>	
TMDS CONN DN<5>	TMDS_CONN_DN<4>	
TMDS CONN DP<5>	TMDS_CONN_DN<3>	
	TMDS_CONN_DP<4>	
	TMDS_CONN_DP<3>	
TMDS_CONN_CLKP	DVI_DDC_CLK_UF	
TMDS_CONN_CLKN	(+5V_DDC SLEEP)	
VGA_B	DVI_DDC_DATA_UF	
VGA_HSYNC	VGA_VSYNC	
	DVI_HPD_UF	
	VGA_R	
	VGA_G	

L45 90-OHM-300mA 2012H CRITICAL — TMDS_DN<0>, TMDS_DP<0> → TMDS_CONN_DN<0>, TMDS_CONN_DP<0>

3V LEVEL SHIFTERS

+3V_SLEEP

Q39 2N7002DW SOT-363: DVI_DDC_CLK ↔ GPU_DVI_DDC_CLK
Q39 2N7002DW SOT-363: DVI_DDC_DATA ↔ GPU_DVI_DDC_DATA
Q40 2N7002DW SOT-363: DVI_HPD ↔ GPU_HPD

R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

L47 / L46 / L44 CRITICAL 90-OHM-300mA 2012H EXT_TMDS

L47	TMDS_CONN_DN<2>	TMDS_DN<4>
	TMDS_CONN_DP<2>	TMDS_DP<4>
L46	TMDS_CONN_DN<1>	TMDS_DN<3>
	TMDS_CONN_DP<1>	TMDS_DP<3>
L44	TMDS_CONN_DN<0>	TMDS_DN<2>
	TMDS_CONN_DP<0>	TMDS_DP<2>

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. since most rails will be low. TP0610 will turn on, giving SOFT_PWR_ON is low. As most rails rise, TP0610 will turn off, and DDC CLK remote device path is DC isolation will be disabled as well.

Q38 TP0610 SM: DVI_DDC_CLK_UF → DVI_DDC_CLK
R473 680 5% 1/16W MF 402: DVI_TURN_ON → DVI_TURN_ON_TLM
R459 330 5% 1/16W MF 402: Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
R460 10K 5% 1/16W MF 402: DVI_TURN_ON_BASE
Q35 MMDT3904 SOT-363: SOFT_PWR_ON_L

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP

R485 68.1K 1% 1/16W MF 402
C668 0.1UF 20% 10V CERM 402
U42 LMC7211 SM: HPD_4V_REF, GPIO
R472 10K 1% 1/16W MF 402: DVI_HPD_UF → DVI_HPD_DIV
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
R475 10K 5% 1/16W MF 402: HPD_PWR_SW_BASE
Q35 MMDT3904 SOT-363
R470 330 5% 1/16W MF 402: HPD_PWR_SW
HPD_REF_EN_L
Q40 2N7002DW SOT-363
R483 470K 5% 1/16W MF 402: HPD_PWR_SNS_EN

L49 / L85 CRITICAL 90-OHM-300mA 2012H EXT_TMDS

L49	TMDS_DN<4>	TMDS_CONN_DN<4>
	TMDS_DP<4>	TMDS_CONN_DP<4>
L85	TMDS_DN<5>	TMDS_CONN_DN<5>
	TMDS_DP<5>	TMDS_CONN_DP<5>

+PBUS INVERTER INTERFACE

L73 FERR-1K-OHM-EMI SM: +14V_INV

+5V_MAIN
Q76 FDG6324L SC70-6: +5V_INV_UF_SW → +5V_INV_SW
R750 100K 5% 1/16W MF 402: FP_PWR_EN_L
Q76 FDG6324L SC70-6: FP_PWR_EN
L74 400-OHM-EMI SM-1
L72 400-OHM-EMI SM-1: BRIGHT_PWM
C813 10UF 20% 6.3V CERM 805
C812 0.001uF 20% 50V CERM 402
C815 0.001uF 20% 50V CERM 402
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
L1 FERR-250-OHM SM
J4 SM-2MT CRITICAL: +5V_INV_SW, INV_GND

+3V_MAIN
C22 0.1UF 10% 16V CERM 402
U2 NC7S32 SC70: INV_ON_PWM → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

LCD INTERFACE

LVDS INTERFACE

+3V_MAIN
LCD POWER SWITCH
R347 100K 5% 1/16W MF 402
C474 2200pF 10% 50V CERM 603
R354 100K 5% 1/16W MF 402: LCD_PWREN_L
Q29 SI3443DV TSOP: +3V_LCD_SW → +3V_LCD
Q28 2N7002 SM: FP_PWR_EN
LCD_DIGON_L
+3V_SLEEP

L27 FERR-250-OHM SM: +3V_LCD_SW → +3V_LCD (LVDS DDC POWER)

C548 0.001uF 20% 50V CERM 402
C503 0.001uF 20% 50V CERM 402
C549 0.001uF 20% 50V CERM 402

J14 G-501973 F-RT-SM CRITICAL

LVDS_DDC_CLK	NC
LVDS_DDC_DATA	LVDS_DDC_CLK
LVDS_L0N	LVDS_DDC_DATA
LVDS_L0P	LVDS_L0N
LVDS_L1N	LVDS_L0P
LVDS_L1P	LVDS_L1N
LVDS_L2N	LVDS_L1P
LVDS_L2P	LVDS_L2N
CLKLVDS_LN	LVDS_L2P
CLKLVDS_LP	CLKLVDS_LN
	CLKLVDS_LP
	NC

R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
LVDS_DDC_CLK
LVDS_DDC_DATA

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C702 0.001uF 20% 50V CERM 402 NO STUFF

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM: GPU_TV_GND1 → L54 FERR-10-OHM-500MA SM → TV_GND1

GPU_Y	L53 3.3uH 0603	C663 560pF 10% 50V CERM 402
GPU_C	L57 3.3uH 0603	C661 560pF 10% 50V CERM 402
GPU_COMP	L55 3.3uH 0603	C664 560pF 10% 50V CERM 402

C657 0.01UF 10% 50V CERM 603
C656 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
C659 0.01UF 10% 50V CERM 603

J21 MINIDIN RT-TH MH11773-WMR8A CRITICAL: TV_C, TV_Y, TV_COMP

XW14 SM: GPU_TV_GND2 → L56 FERR-10-OHM-500MA SM → TV_GND2

Place GND shorts at graphics controller

CHGND1

VIDEO CONNECTORS

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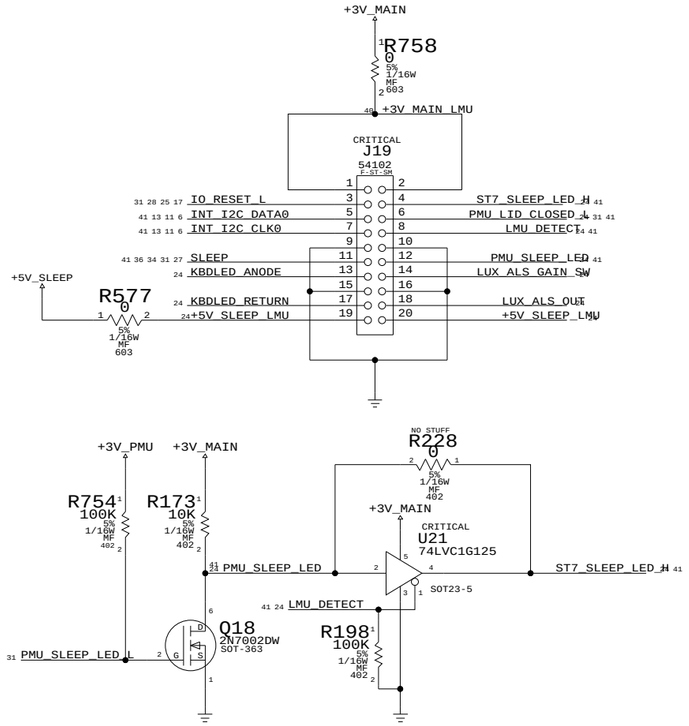
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

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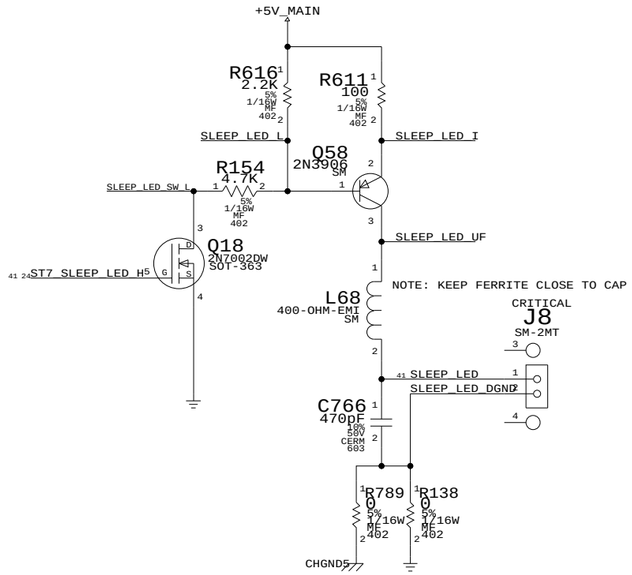
SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 23 OF 46	

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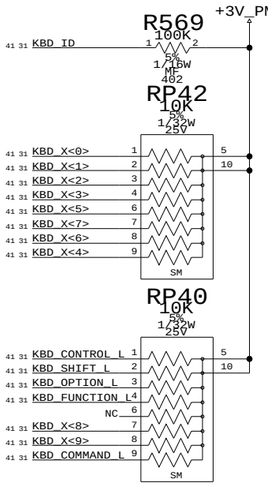
LMU/RIGHT SENSOR CONNECTOR



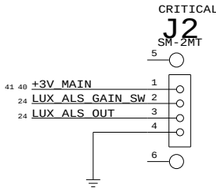
SLEEP LED

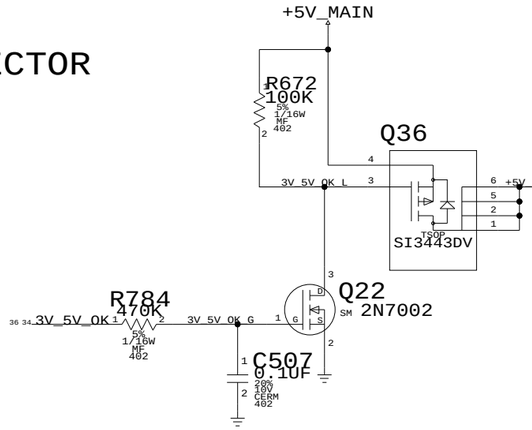


KEYBOARD PULLUPS

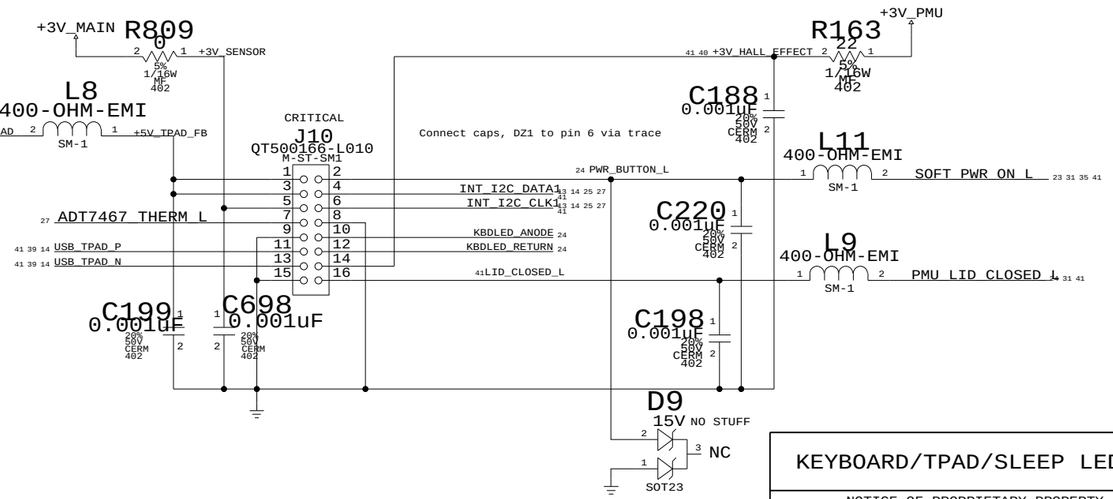


LEFT LIGHT SENSOR CONNECTOR

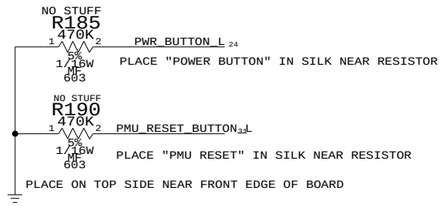




USB Trackpad Connector



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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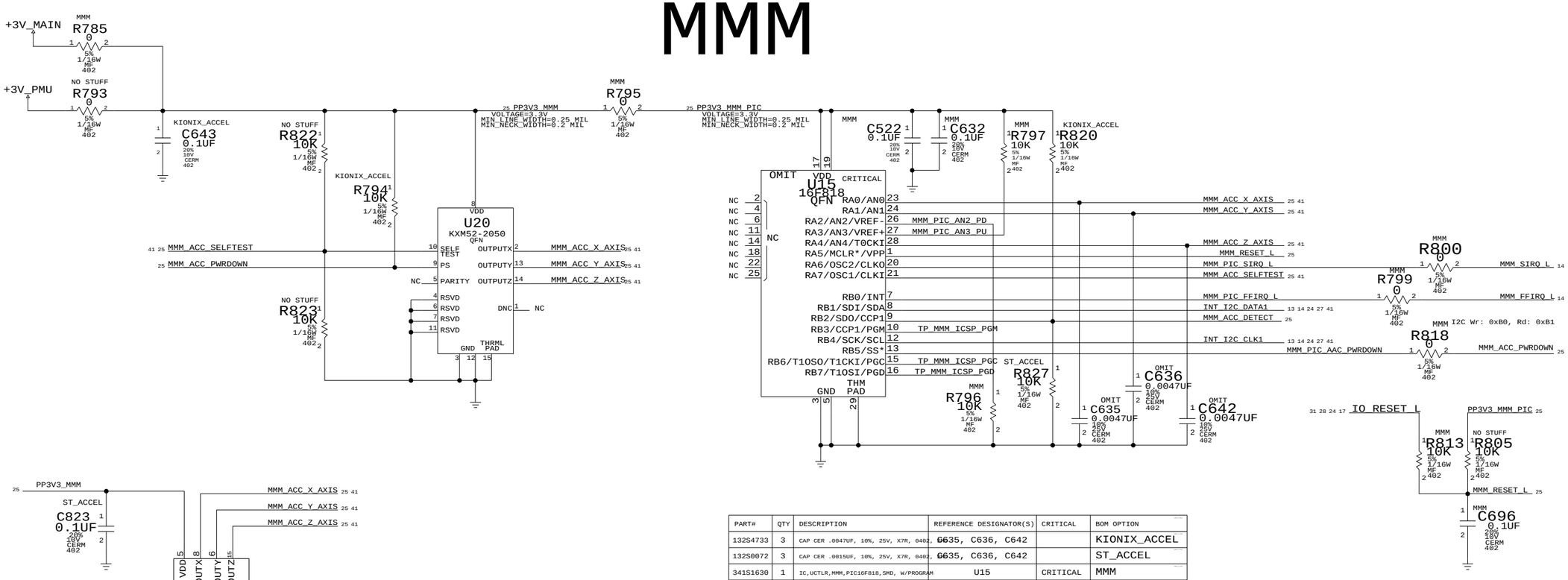
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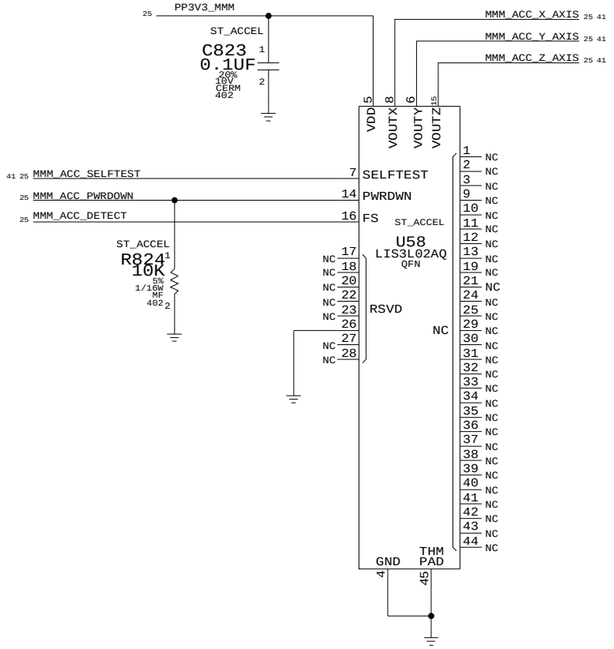
SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT	OF
NONE	24	46

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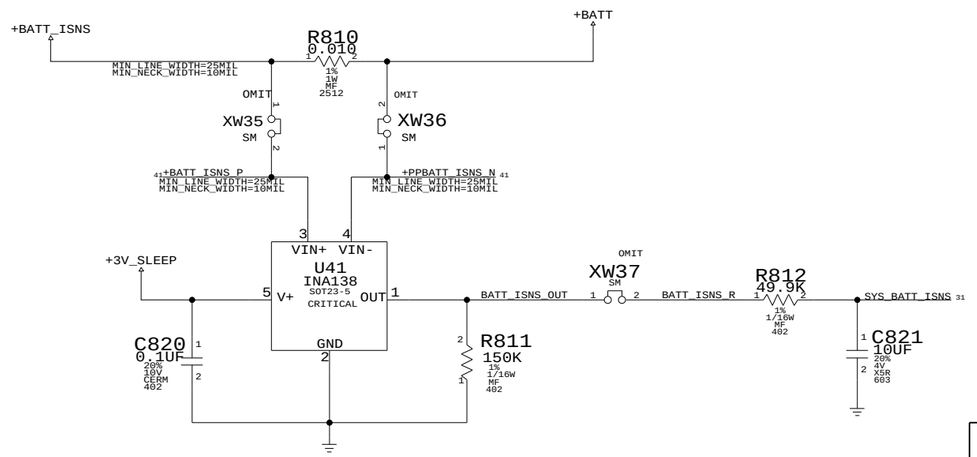
MMM





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S4733	3	CAP CER .0047UF, 10%, 25V, X7R, 0402,	C635, C636, C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402,	C635, C636, C642		ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD, W/PROGRAM	U15	CRITICAL	MMM

BATTERY CURRENT SENSE



MMM & BATTERY CURRENT SENSOR

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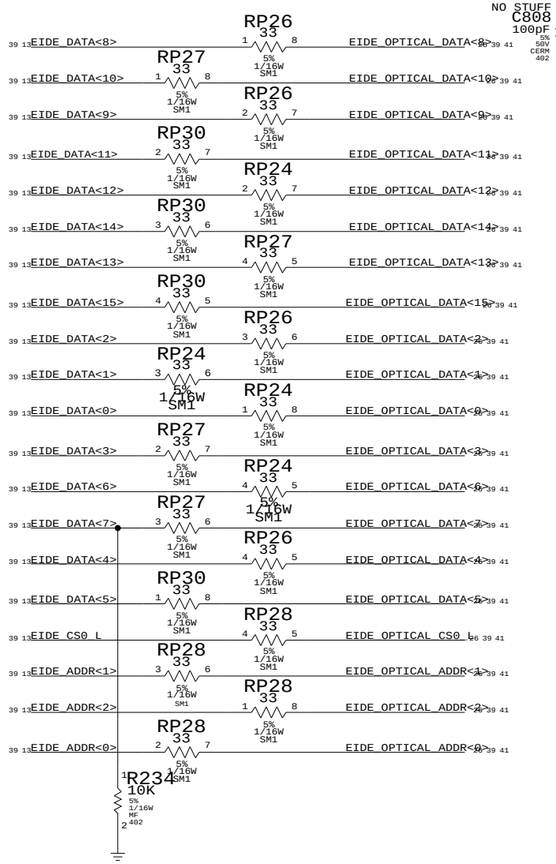
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 25 OF 46	

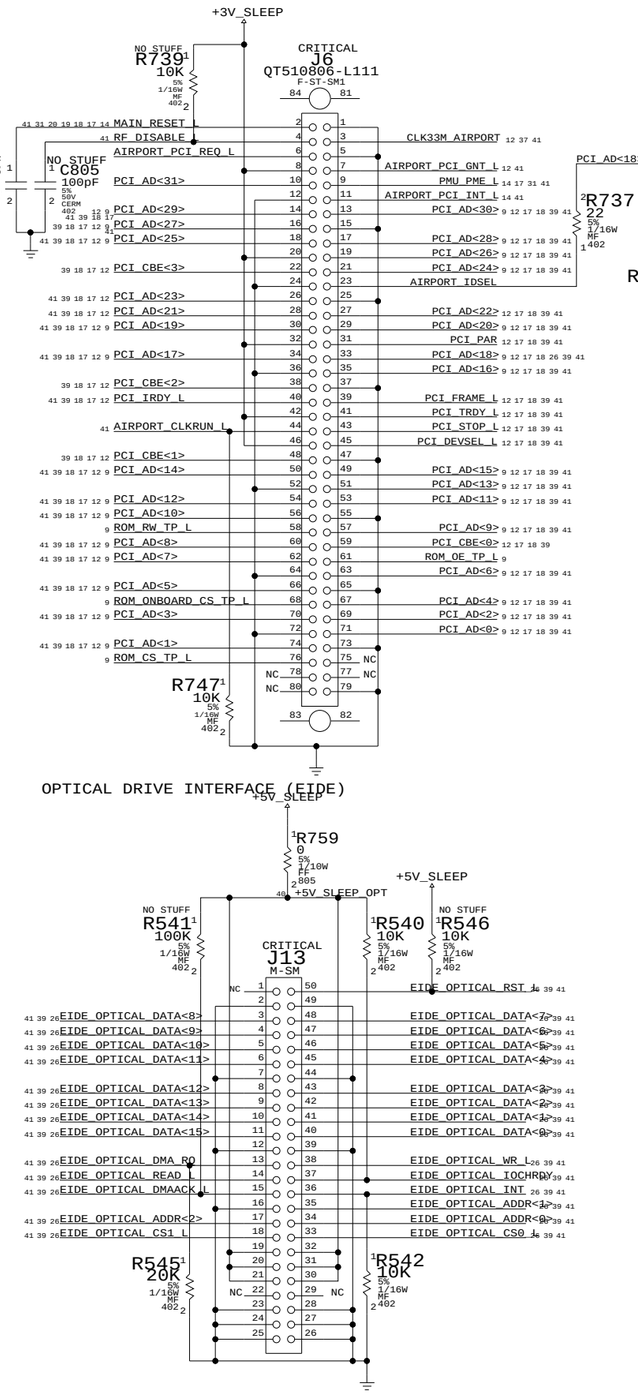
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WIRELESS INTERFACE

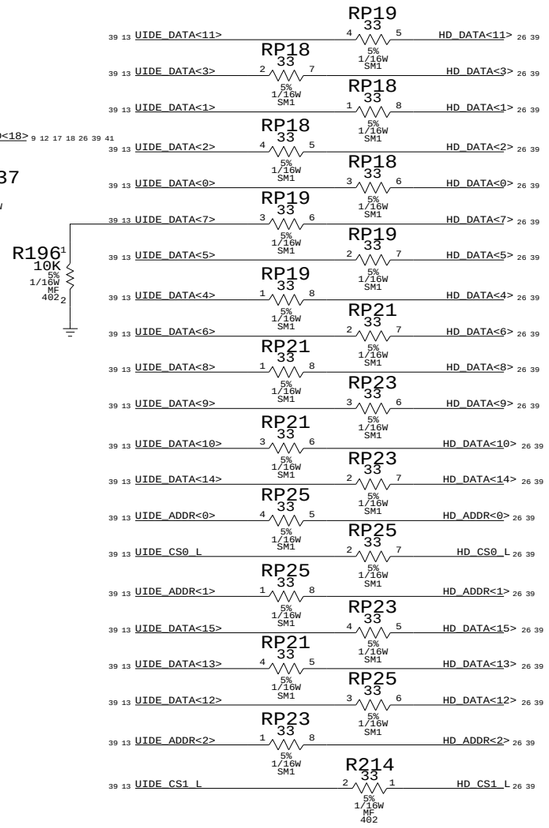
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID



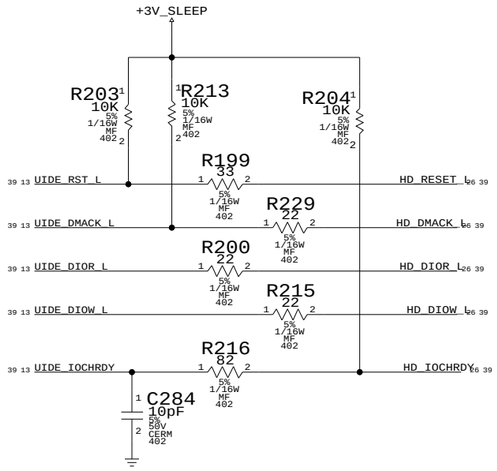
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

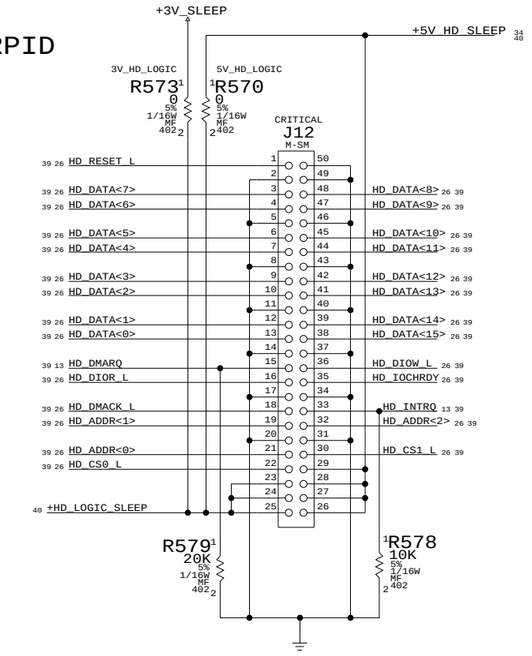


PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

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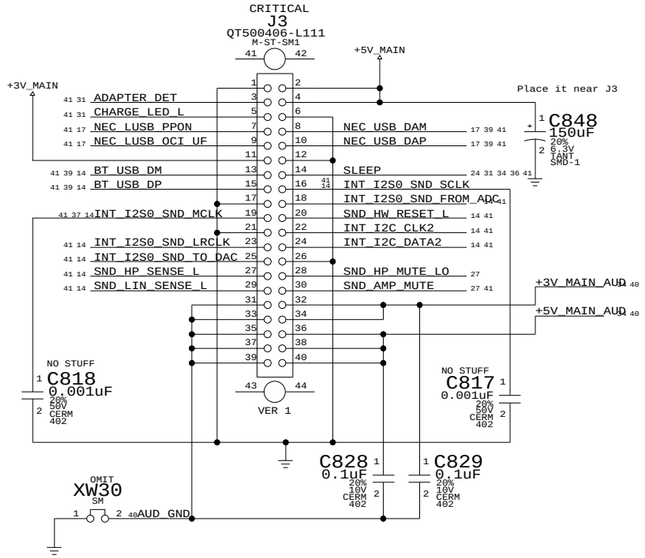
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

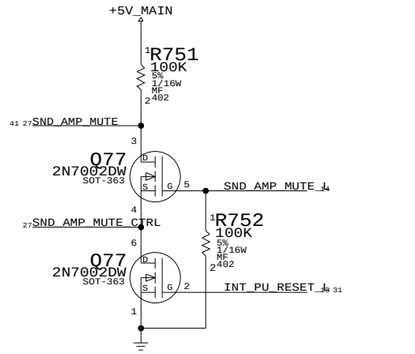
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 26 OF 46	

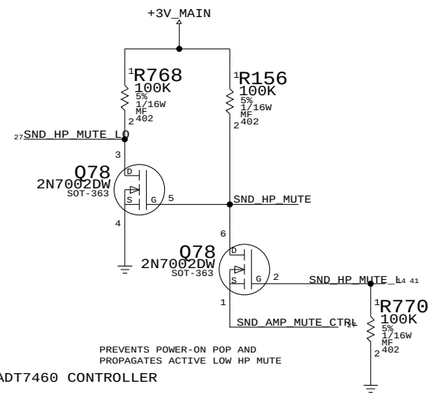
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LEFT I/O & AUDIO BOARD (LIO)



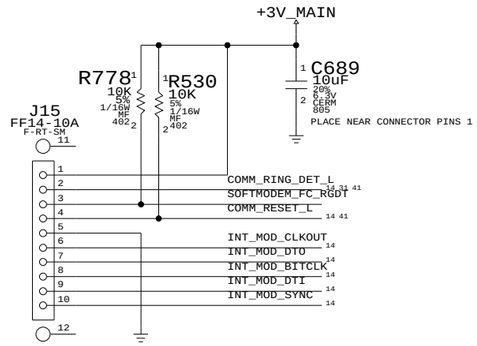


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE

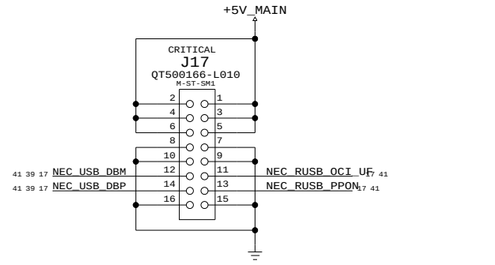


PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

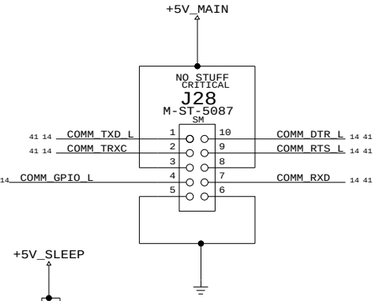
SOFT MODEM CONN



RIGHT USB BOARD



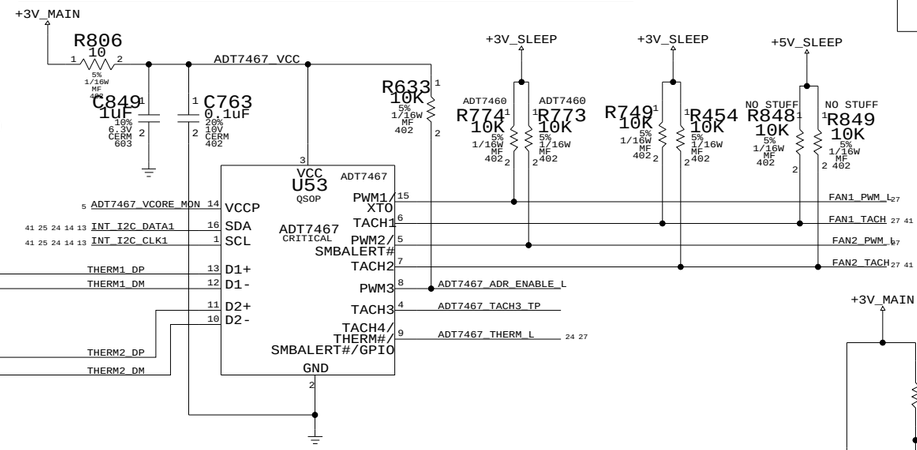
SERIAL DEBUG INTERFACE



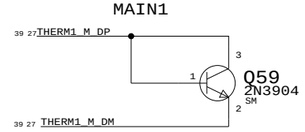
FAN INTERFACE

FAN CONTROLLER

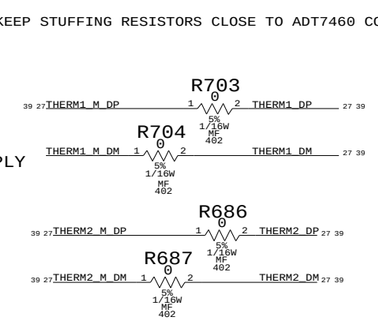
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0608	1	IC,ADT7460,FAN CTLR,16P QSOP	U53	CRITICAL	ADT7460



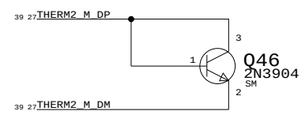
PLACE CLOSE TO CPU
MAIN1



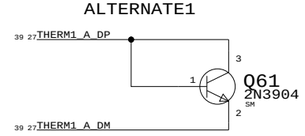
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



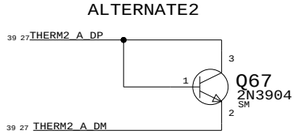
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



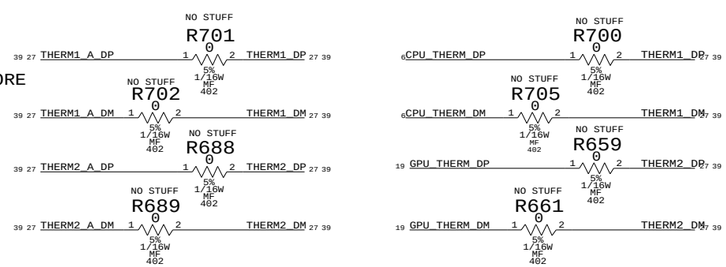
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



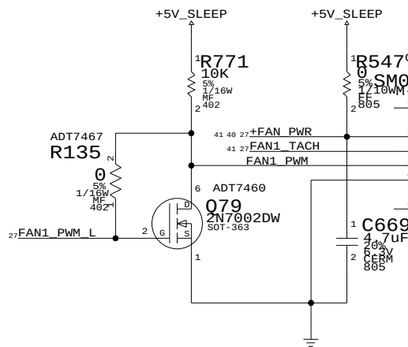
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



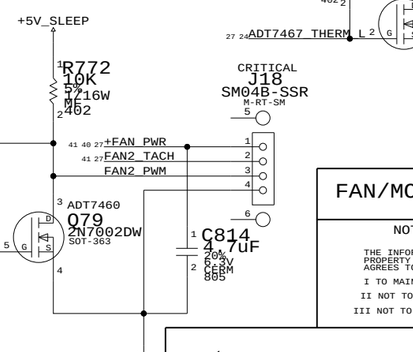
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

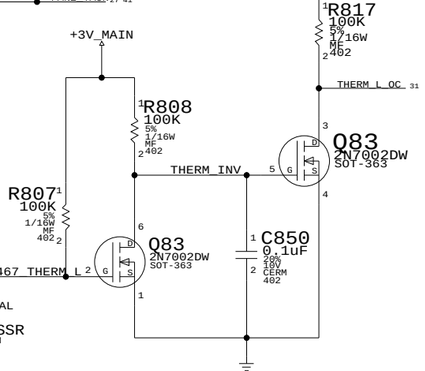


CPU FAN



GPU FAN





FAN/MODEM/SOUND/BACKUP BATT.

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 27 OF 46	

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079		U43	MARVELL 88E1111 B1 DIE

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

NO STUFF R513 0 5% 1/16W MF 402

C680 10uF 20% 6.3V CERM 805

U45 LTC3405 SOT23-6 CRITICAL

3405_MODE

R507 0 5% 1/16W MF 402

LTC3405_SW

CRITICAL L60 3.3uH SM1

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

C674 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

3405_VFB

R503 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX — CLKENET_PHY_TX

R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX — CLKENET_PHY_RX

R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF — CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402 — C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

U43 88E1111 BCC CRITICAL

TX_CLK, RX_CLK, 125CLK, TXD0–TXD7, TX_EN, TX_ER, GTX_CLK, RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO, INT-/INT+, RESET, COMA, S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-, XTAL1, XTAL2, VSSC, GND

CTRL10, NC, DVDD, VDDO, VDDOH, VDDOX, AVDD

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

CONFIG0–CONFIG6

TDI, TDO, TCK, TMS, TRST

RSET, SEL_OSC, SEL_2.5V

C594 C601 C608 C619 C603 C599 — 0.1uF / 0.01uF / 0.1uF / 0.01uF / 0.1uF / 0.01uF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C597 C612 C623 C600 C598 C595 — 0.1uF / 0.01uF / 0.1uF / 0.01uF / 0.1uF / 10uF 20% 10V CERM 402 / 805

+2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C614 C616 C618 C602 C592 — 0.1uF / 0.1uF / 0.1uF / 0.01uF / 10uF 20% 10V CERM 402 / 805

+2_5V_MARVELL_AVDD

L35 FERR-EMI-600-OHM SM

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN

R442 0 5% 1/10W FF 805

C646 C648 C645 C647 — 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

R814 0 5% 1/10W FF 805

+2_5V_MARVELL_CONN

J23 MJ-R0076 F-RT-TH

PRIMARY

ENET_CTAP, ENET_CTAP, MDI_0+, MDI_0-, MDI_1+, MDI_1-, MDI_2+, MDI_2-, MDI_3+, MDI_3-

1CT:1CT, 75 OHM

SECONDARY J1 J2 J3 J4 J5 J6 J7 J8

RJ45 CABLE SIDE

RJ45 CHIP SIDE

CHGND1

SHIELD 1000PF, 2000V

+2_5V_MARVELL

R431 10K 5% 1/16W MF 402

R430 10K 5% 1/16W MF 402

R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402

INT_ENET_RST_L

D15 1N914 SOT23

IO_RESET_L

ENET_RST_L

ENET_COMA

C611 2.2uF 10% 10V CERM 805

Q32 2N7002DW SOT-363

AC_IN

SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

ENET_HSDACP, ENET_HSDACM

CLK25M_ENET_XIN, CLK25M_ENET_XOUT

ENET_VSSC

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M

C604 27pF 5% 50V CERM 402

C624 27pF 5% 50V CERM 402

CLK25M_XTAL_IN

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402

R429 49.9 1% 1/16W MF 402

R428 10K 5% 1/16W MF 402

R427 4.99K 1% 1/16W MF 402

R433 R435 R437 R439 — 49.9 1% 1/16W MF 402

R434 R436 R438 R440 — 49.9 1% 1/16W MF 402

MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C622 C613 C615 C617 — 0.01uF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

LED_LINK10, LED_LINK100, LED_RX_SPN

SEE CONFIG TABLES (BELOW)

ENET_ENERGY_DET, ENET_RSET, INT_TDO, JTAG_ASIC_TDO_TP, JTAG_ASIC_TCK, JTAG_ASIC_TMS, JTAG_ASIC_TRST_L

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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165MA MAX LOAD

D25 SC-59 SDM20E40C

U37 LM2594 SM — CRITICAL — VIN, FB, VOUT, GND ON/OFF — L59 220uH SM-3 — +3V_FW_UF

C665 10uF 20% 50V CERM 2320 — D16 SM MBR0540 — C670 100uF 20% 6.3V POLY CASE-B-3528

L34 400-OHM-EMI SM-1 — R414 10 5% 1/16W MF 603 — +1.95V_FW_DVDD

C587 0.1uF 20% 10V CERM 402 — C684 0.1uF 20% 10V CERM 402 — C585 2.2uF 20% 10V CERM 805 — PHY PINS 72,76

C588 2.2uF 20% 10V CERM 805 — C589 0.1uF 20% 10V CERM 402 — PHY PIN 64

U44 LTC1761ES5-BYP SOT-23-1 — CRITICAL — VOUT = 1.22*(1+R2/R1)+ IADJ*R2, IADJ = 30NA AT 25C

C671 2.2uF 20% 10V CERM 805 — C610 0.01uF 20% 16V CERM 402 — R496 16.2K 1% 1/16W MF 402 R2 — R495 27.4K 1% 1/16W MF 402 R1 — C609 10uF 20% 6.3V CERM 805

R418 1 5% 1/16W MF 603 — +3V_FW_AVDD_PORT2 — C593 1uF 20% 10V CERM 603 — PHY PIN 61

R426 1 5% 1/16W MF 603 — +3V_FW_AVDD_PORT1 — C606 1uF 20% 10V CERM 603 — PHY PIN 59

R420 1 5% 1/16W MF 603 — +3V_FW_AVDD_PORT0 — C596 1uF 20% 10V CERM 603 — PHY PIN 40

R413 1 5% 1/16W MF 603 — +3V_FW_AVDD — C584 1uF 20% 10V CERM 603 — PHY PIN 21

R415 3.3 5% 1/16W MF 603 — R416 3.3 5% 1/16W MF 603 — +1.95V_FW_PLLVDD — +1.95V_FW_PLL500VDD — +1.95V_FW_PLL400VDD

C586 1uF 20% 10V CERM 603 — PHY PIN 25 — C678 1uF 20% 10V CERM 603 — PHY PIN 28

R419 1 5% 1/16W MF 603 — +1.95V_FW_DVDD — R417 1 5% 1/16W MF 603 — +1.95V_FW_DVDD_RX0 — +1.95V_FW_DVDD_TX0

C591 0.1uF 20% 10V CERM 402 — PHY PIN 38 — C590 0.1uF 20% 10V CERM 402 — PHY PIN 38

R519 22 5% 1/16W MF 402 — FW_PHY_CNTL<0> — FW_LINK_CNTL<0>

R520 22 5% 1/16W MF 402 — FW_PHY_CNTL<1> — FW_LINK_CNTL<1>

R518 22 5% 1/16W MF 402 — CLKFW_PHY_PCLK — CLKFW_LINK_PCLK

C681 10uF 20% 6.3V CERM 805 — C683 0.1uF 20% 10V CERM 402 — C677 0.1uF 20% 10V CERM 402 — C676 0.1uF 20% 10V CERM 402 — C682 0.1uF 20% 10V CERM 402 — PHY PINS 4,14

U38 LT1962-ADJ MSOP — CRITICAL — IN, OUT, NC, NC, ADJ, BYP, SHDN, GND — FW_CORE_ADJ — FW_CORE_BYP

C625 2.2uF 20% 10V CERM 805 — C621 0.01uF 10% 16V CERM 402 — R443 16.2K 1% 1/16W MF 402 R2 — C620 10uF 20% 6.3V CERM 805 — R444 27.4K 1% 1/16W MF 402 R1

R509 1K 5% 1/16W MF 402 — R505 1K 5% 1/16W MF 402 — R497 1K 5% 1/16W MF 402 — R515 1K 5% 1/16W MF 402 — R508 0 5% 1/16W MF 402

U36 TSB81BA3A PQFP (SYM_VER1) — CRITICAL — SN0201029PFP

AVDD 3.3 — DVDD 1.8 — DVDD 3.3 — PLL VDD 1.8 — PLL VDD 3.3 — AGND — DGND — PLLGND

DS0, DS1, LCLK, LPS, LREQ, PC0, PC1, PC2, PD, BMODE, CPS, D0–D7, RESETZ, SE, SM, TESTM, VREG_PD, THRML PAD, PCLK, PINT, CNA, CTL0, CTL1, (DS2) C/LKON, TPA0+/-, TPA1+/-, TPA2+/-, TPB0+/-, TPB1+/-, TPB2+/-, TPBIAS0, TPBIAS1, TPBIAS2, XI, XO, R0, R1, 31TX0

FW_PORT1_SEL — CLKFW_PHY_LCLK — FW_PHY_LPS — FW_PHY_LREQ — PWR CLASS = 100 (MAY PROVIDE POWER, OR MAY REQUIRE UP TO 5W) (PC0 IS MSB, PC2 IS LSB) — FW_PC_PU — FW_PC_PD — 1MA (MAX) BUS HOLDERS — FW_PHY_PD — FW_BMODE — FW_CPS — FW_PHY_RESET_L — FW_INPUT_PD — FW_TESTM — FW_VREG_PD

CLKFW_PHY_PCLK — FW_PINT — FW_PHY_CNTL<0> — FW_PHY_CNTL<1> — FW_LKON

R502 402K 1% 1/16W MF 402 — +FW_PWR_OR

RP38 22 5% 1/16W SM1 — RP37 22 5% 1/16W SM1 — FW_LINK_DATA<0:7> — FW_PHY_DATA<0:7>

R505 1K 5% 1/16W MF 402 — R515 1K 5% 1/16W MF 402 — R517 1K 5% 1/16W MF 402 — R514 1K 5% 1/16W MF 402 — C679 0.22uF 20% 6.3V CERM 402 — R500 470 5% 1/16W MF 402 — R501 1K 5% 1/16W MF 402 — R486 1K 5% 1/16W MF 402

R516 10K 5% 1/16W MF 402 — CLKFW_PHY_PCLK

R488 56.2 1% 1/16W MF 402 — R487 56.2 1% 1/16W MF 402 — C605C607 1uF 20% 10V CERM 603 — 1uF 20% 10V CERM 603 — R492 56.2 1% 1/16W MF 402 — R491 56.2 1% 1/16W MF 402

FW_TPA0P — FW_TPA0N — (FWB-RX) — FW_TPA1P — FW_TPA1N — (FWA-RX)

FW_TPB0P — FW_TPB0N — (FWB-TX) — FW_TPB1P — FW_TPB1N — (FWA-TX)

R510 47 5% 1/16W MF 402 — FW_XI — FW_OSC

CRITICAL — VCC, G2 98.304MHZ OSC SM-A, OUT, OE, GND — +3V_FW — FW_OSC_EN

NO STUFF R412 100K 5% 1/16W MF 402

R511 100 5% 1/16W MF 402 — FW_R0 — FW_R1

C583 0.22uF 20% 6.3V CERM 402

R512 6.34K 1% 1/16W MF 402

R494 56.2 1% 1/16W MF 402 — R493 56.2 1% 1/16W MF 402 — R490 56.2 1% 1/16W MF 402 — R489 56.2 1% 1/16W MF 402

FWB_TPB0 — FWB_TPB1

C673 220pF 5% 25V CERM 402 — R499 4.99K 1% 1/16W MF 402 — C672 220pF 5% 25V CERM 402 — R498 4.99K 1% 1/16W MF 402

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

DSx Strap Options
0 = Bilingual port
1 = A-only port

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

FIREWIRE PHY

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PORT POWER SWITCH

+PBUS
F3 1.5A-24V SM
+FW_PBUS
CRITICAL Q34 NDS9407 SOI
+FW_SW
CRITICAL D24 SMB B340B
+FW_PWR_OR
R448 470K 5% 1/16W MF 402
C639 0.01UF 20% 16V CERM 402
FW_GATE_EN
+3V_PMU
R447 100K 5% 1/16W MF 402
DP6 BAS16TW SOT-363
POWER_UP
Q33 2N7002DW SOT-363
PMU_POWER_UP_L
R461 330K 5% 1/16W MF 402
FW_GATE_EN_RC
Q33 2N7002DW SOT-363
FW_POWER_UP
R803 0 5% 1/16W MF 402
DCDC_EN
DCDC_EN_CTRL
DP6 BAS16TW SOT-363
R446 10K 5% 1/16W MF 402
AC_IN
AC_IN_FW_CNTL
DP6 BAS16TW SOT-363
R777 470K 5% 1/16W MF 402

ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

+3V_FW
R451 10K 5% 1/16W MF 402
+3V_FW_ESD_ITM
L39 400-OHM-EMI SM-1
NO STUFF C822 0.1UF 20% 16V CERM 402
C630 0.1UF 20% 16V CERM 402
C637 0.001UF 20% 50V CERM 402
D21 1N5227B SOT23
C638 0.01UF 20% 16V CERM 402
+3V_FW_ESD
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
C633 0.01UF 20% 16V CERM 402

L76 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
FW_TPO0P
FW_TPO0N
L77 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
FW_TPI0P
FW_TPI0N
(AREF)
(BREF)
(TPI0R)
FW_VGND0
NC
FW_VP0
CRITICAL J20 1394B F-RT-SM
INT-SHIELD
TPA
TPA(R)
TPA*
VG
SC
VP
TPB
TPB(R)
TPB*
INT-SHIELD
C650 0.01UF 20% 16V CERM 402
CHGND1

PORT 0
1394a/b
(BILINGUAL)
514S0058

L51 FERR-250-OHM SM

R465 1M 5% 1/16W MF 402
C649 0.1uF 20% 50V CERM 805
NO STUFF C652 0.01uF 20% 16V CERM 402
R466 0 5% 1/10W MF 805
NO STUFF C651 0.01uF 20% 16V CERM 402
CHGND1

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

R837 0 5% 1/16W MF 603
+FW_PWR_OR_F
PLACE NEAR D24
Q37 NO STUFF SI2319DS SOT23
NO STUFF R829 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE
NO STUFF R830 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE_L
NO STUFF R831 649K 1% 1/16W MF 402
NO STUFF Q73 2N7002 SM
+FW_PWR_CTRL
NO STUFF C824 1UF 20% 10V CERM 603
NO STUFF D35 SM MBR0540
+2_5V_REG_F
NO STUFF C825 0.1UF 20% 10V CERM 402
NO STUFF U59 LMC7211 SM
+3V_FW_ESD_R
NO STUFF R834 10K 5% 1/16W MF 402
+3V_FW_ESD
NO STUFF R835 102K 1% 1/16W MF 402
2.5V REG
NO STUFF C826 0.01UF 20% 16V CERM 402
NO STUFF R836 332K 1% 1/16W MF 402
PLACE NEAR D23
NO STUFF R833 604K 1% 1/16W MF 402

2.5V REG: 2.50V - 2.15V
200MS - 500MS

F1 1.5AMP-33V SM
+FW_PWR1
L58 FERR-250-OHM SM

+3V_FW_ESD
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
C640 0.01UF 20% 16V CERM 402
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
C644 0.01UF 20% 16V CERM 402

PORT 1
1394a ONLY
514-0057

L52 260-OHM-330MA SM1 SYM_VER-2
FW_TPA1P
FW_TPA1N
L48 260-OHM-330MA SM1 SYM_VER-2
FW_TPB1P
FW_TPB1N
CRITICAL J24 1394A F-RT-TH
FW_TPO1P
FW_TPO1N
FW_TPI1P
FW_TPI1N
FW_VP1
FW_VGND1
TPO
TPO#
TPI
TPI#
VP
VGND

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

R471 0 5% 1/10W MF 805
C662C666 0.01uF 0.01uF 20% 16V CERM 402
CHGND1

R816 0 5% 1/16W MF 402 EMI
CHGND1

FIREWIRE PORTS

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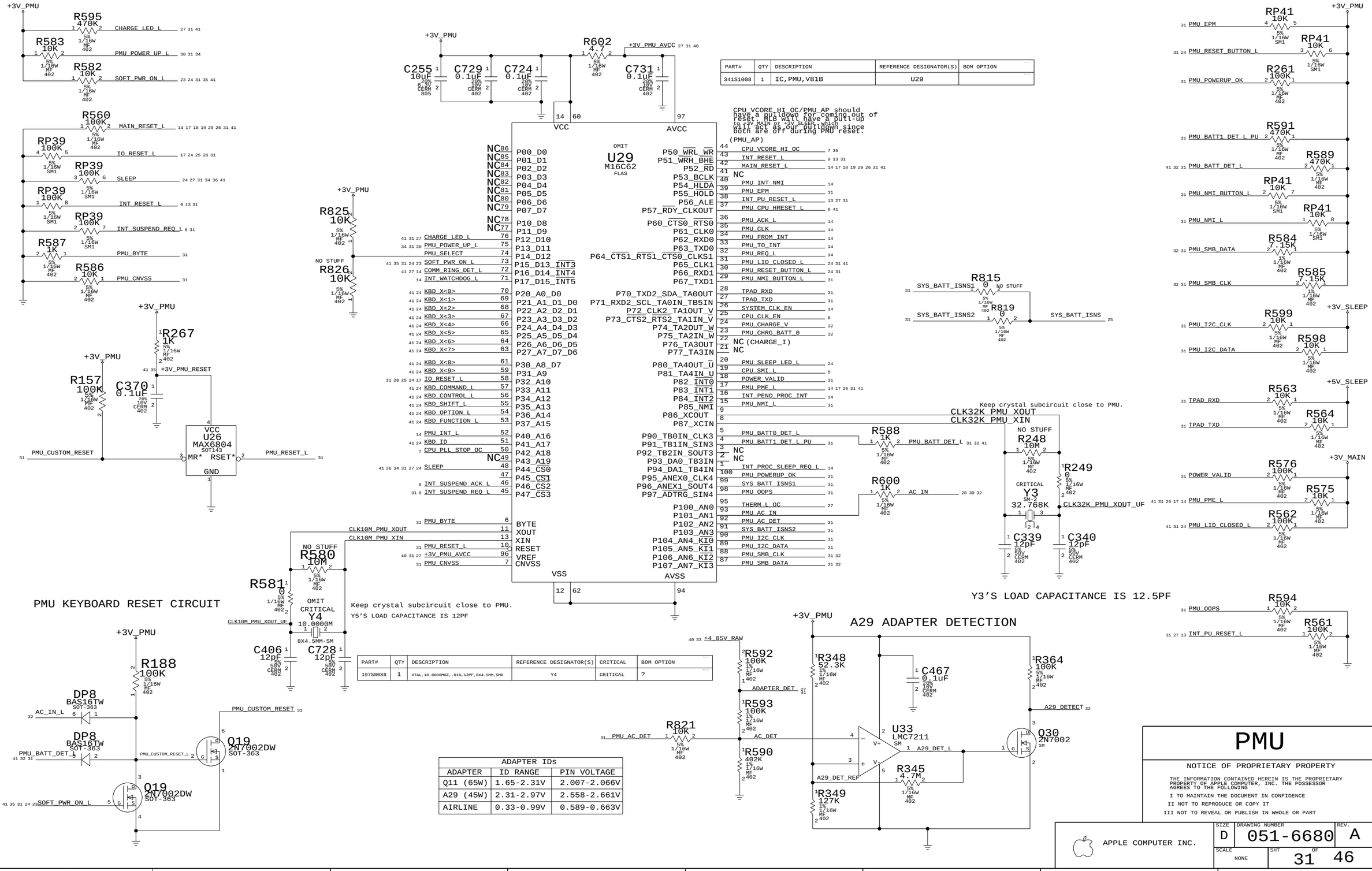
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DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

41 40 33 +ADAPTER

C35 0.1uF 20% 16V CERM X7R 603-1

GREATER THAN 13.1V DETECT

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/16W MF 402

C11 0.1uF 20% 50V CERM 805

AC ENABLE GATE

R51 20K 1% 1/16W MF 402

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/16W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

40 33 1V20_REF

U1 LMC7211 SM

AC_DIV

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

R41 1M 5% 1/16W MF 402

AC_IN 28 30 31 32

AC_IN_L 31 32

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

Q1 2N7002DW SOT-363

BACKFEED PROTECTION

40 +ADAPTER_SW

Q69 SI4435DY SOI

+ADAPTER_SENSE 40

BKFD_PROT_GATE

C803 0.01UF 20% 16V CERM 603

R734 68K 5% 1/16W MF 402

BKFD_PROT_EN_L

32 31 30 28 AC_IN

Q9 2N7002DW SOT-363

CRITICAL
U3 MAX4172 TSSOP

RS+ RS- PG OUT GND

NC NC NC1 NC2

MAX4172_OUT 2

CRITICAL
R77 2.21K 0.1% 1/16W MF 603-2

+24V_PBUS

C36 0.01uF 20% 50V CERM 603

C233 0.1uF 10% 50V X7R 603-1

Place close to RS-

PLACE U24 NEXT TO R382

CRITICAL
R61 0.025 1% 1W MF 2512

R57 100K 1% 1/16W MF 402

D4 1N914 SOT23

R82 4.7 5% 1/16W MF 402

R87 4.7 5% 1/16W MF 402

39 1772_CSSP

39 1772_CSSN

C67 1uF 20% 50V CERM 1210

C71 0.47uF 20% 50V CERM 1206

C95 0.47uF 20% 50V CERM 1206

R49 12.7K 1% 1/16W MF 402

40 1772_DCIN

CSSP CSSN

U6 MAX1772 QSOP

DCIN CELLS 1772_CELLS

ACIN LDO

32 1772_ACOK_L ACOK DLOV 1772_DLOV

(+3V_PMU) RFIN BST 1772_BST

1772_VCTL VCTL DHI 1772_DHI

1772_ICTL ICTL LX 1772_LX

1772_ICHG ICHG DLO 1772_DLO

1772_IINP IINP PGND (GND)

1772_CCV CSIP 1772_CSIP

1772_CCI CSIN 1772_CSIN

1772_CCS CCS BATT

REF CLS GND

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

C41 1uF 20% 25V CERM 1206

1772_CCV_RC

1772_REF

C24 0.1uF 20% 16V CERM 402

C23 1uF 20% 16V CERM 603

R54 10K 1% 1/16W MF 402

R53 4.12K 1% 1/16W MF 402

1772_CLS

R83 1K 1% 1/16W MF 402

R55 1K 1% 1/16W MF 402

R56 1K 1% 1/16W MF 402

R94 100K 5% 1/16W MF 402

40 1772_GND

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

1 IAC_RC_COMP

C798 0.1uF 20% 16V CERM 402

+3V_PMU

C794 0.1uF 20% 16V CERM 402

R745 47.2K 0.1% 1/16W TF 603

IAC_FB

U55 LMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

R727 10K 1% 1/16W MF 402

MAX4172_OUT 2

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP 33

ADAPTER_I_REG

CURRENT_THRESHOLD

CRITICAL
R736 42.2K 0.1% 1/16W TF 603

CRITICAL
R738 82.5K 0.1% 1/16W TF 603

CRITICAL
R742 51.1K 0.1% 1/16W TF 603

A29_CURRENT_ADJ

R744 100K 5% 1/16W MF 402

OVER_18V_ADJ

3V_PMU

Q2 2N7002DW SOT-363

32 31 A29_DETECT

Q74 2N7002DW SOT-363

AC_GTR_18V

C809 1uF 20% 16V CERM 603

32 1772_ACOK_L

Q74 2N7002DW SOT-363

BATTERY SWITCH-OVER CIRCUIT

+BATT

+24V_PBUS

F5 5AMP-125V SM-2

+PBUS

F4 5AMP-125V SM-2

40 32 +BATT_24V_FUSE

40 +BATT_14V_FUSE

CRITICAL
Q6 SI4435DY SOI

CRITICAL
Q7 SUD45P03 TO-252

R716 47K 5% 1/16W MF 402

R710 47K 5% 1/16W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

DP1 BAS16TW SOT-363

BATT_24PBUS_EN 5

2 BATT_14PBUS_EN

32 31 AC_IN_L

DP1 BAS16TW SOT-363

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

C118 10uF 20% 6.3V CERM 805

AC_IN_L_RC

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

R731 1K 1% 1/16W MF 402

BATT_LOW_L

BATTV_HIGH

R59 100K 5% 1/16W MF 402

Q4 2N7002DW SOT-363

R75 5.23K 1% 1/16W MF 402

BATTV_LOW 2

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

31 PMU_CHARGE 5

Q4 2N7002DW SOT-363

+3V_PMU

R741 100K 5% 1/16W MF 402

CHARGE_DISABLE 2

Q72 2N7002DW SOT-363

31 PMU_CHRG_BATT_0 5

Q72 2N7002DW SOT-363

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+3V_PMU

C799 0.1uF 20% 16V CERM 402

U57 LMC7211 SM

BATT_LOW 1

R729 100K 1% 1/16W MF 402

R740 499K 1% 1/16W MF 402

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

32 31 A29_DETECT 5

Q2 2N7002DW SOT-363

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

41 40 +BATT_POS

(BATT_IN_PD)

41 BATT_CLK

41 BATT_DATA

PMU_BATT_DET 41

41 40 BATT_NEG

40 +BATT_VSNS

L5 FERR-EMI-100-OHM SM

L2 FERR-50-OHM SM

+BATT_ISNS

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK 41

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA 41

1772_LDO

R725 33 5% 1/8W FF 1206

D6 1N914 SOT23

1772_BST_ESR

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

+24V_PBUS

C96 0.1uF 20% 50V CERM 805

CRITICAL
Q70 IRF7805 SM

C112 2.2UF 20% 6.3V X7R 1206

C117 2.2UF 20% 6.3V X7R 1206

C113 2.2UF 20% 6.3V X7R 1206

C115 2.2UF 20% 6.3V X7R 1206

C116 2.2UF 20% 6.3V X7R 1206

CRITICAL
L70 10uH SM1

+BATT_RSNS 40

R715 0.05 1% 1W MF 2512

+BATT_24V_FUSE 40

D36 SM MBRS140T3

CRITICAL
Q64 IRF7811W SO-8

NO STUFF
C853 1000pF 10% 25V X7R 402

R720 1 5% 1/16W MF 603

R713 1 5% 1/16W MF 603

C780 4.7UF 20% 25V CERM 1206

C777 4.7UF 20% 25V CERM 1206

C795 4.7UF 20% 25V CERM 1206

C792 4.7UF 20% 25V CERM 1206

C790 4.7UF 20% 25V CERM 1206

C785 4.7UF 20% 25V CERM 1206

C779 33uF 20% 25V TANT EEC SM1

XW1 SM

BATTERY CHARGER

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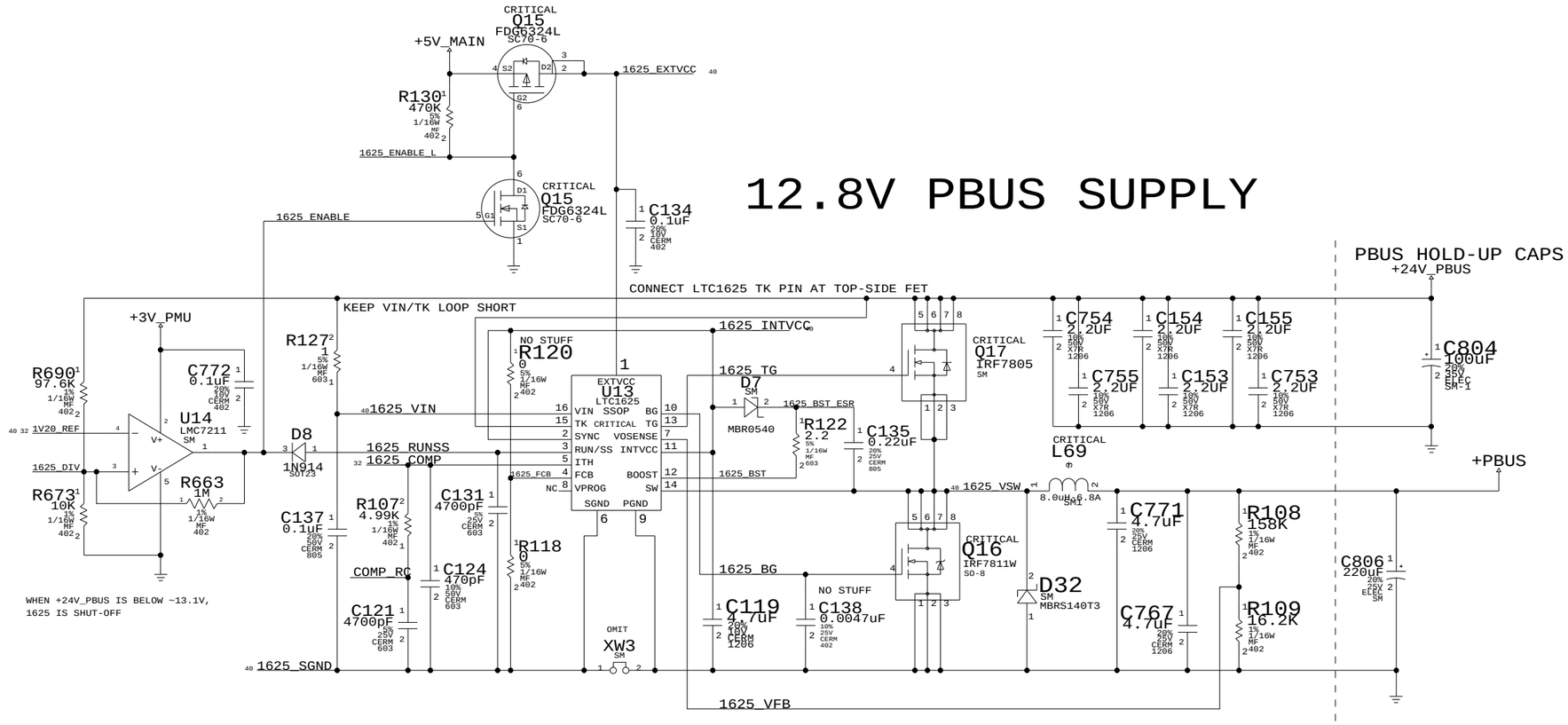
SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE: NONE

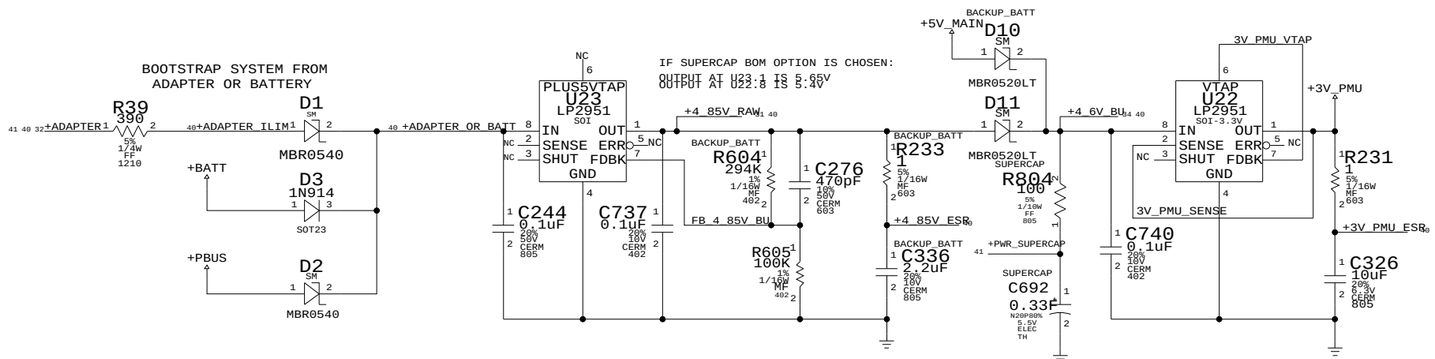
SHT 32 OF 46

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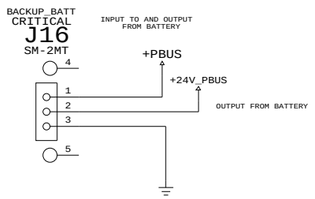
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP

12.8V REGULATOR

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3.3V/5V MAIN SUPPLY

+24V_PBUS

+5V_MAIN

+3V_MAIN

+5V_MAIN_AUD

+3V_MAIN_AUD

5V_RSNS

3V_RSNS

5V_BOOST_ESR

3V_BOOST_ESR

3707_INTVCC

5V_TG

3V_TG

5V_BOOST

3V_BOOST

5V_SW

3V_SW

5V_BG

3V_BG

5V_SNSP

3V_SNSP

5V_SNSM

3V_SNSM

5V_VOSNS

3V_VOSNS

5V_ITH

3V_ITH

5V_RUNSS

3V_RUNSS

5V_ITH_RC

3V_ITH_RC

3707_FSET

3707_FCB

3707_STBY

3707_SGND

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L

3V START TO TURN ON ~25MS AFTER DCDC_EN_L

DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN

POWERDOWN DELAY IS AROUND 4MS-15.6MS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

+4_6V_BU

DCDC_EN_L

LTC3707_START_RC

3V_5V_OK

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

SLEEP_L_LS5_NET

SLEEP_LS5_NET

SLEEP_NET

SLEEP_L_LS5

SLEEP_LS5

SLEEP_L_LS5_EN_L

SLEEP_LS5_EN_L

SLEEP

+3V_SLP_OK

+3V_SLP_ON

5V_HD_PWREN

5V_HD_SLEEP

5V_SLEEP_PWREN

3V_SLEEP_PWREN_L

SLEEP_NET_INV

3.3V/5V REGULATOR

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NONE	34	46

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.67GHZ (1.28VCORE) 1.300V->0.975V

1.50GHZ 1.200V->0.975V

1.67GHZ (1.26VCORE) 1.300V->0.975V

(VALUE WITHOUT OFFSET)

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of core

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V = VA. B

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.67GHZ 1.320V->0.990V (CPU SPEC: 1.280V -> 0.980V)

1.50GHZ 1.240V->0.990V (CPU SPEC: 1.200V -> 0.980V)

1.67GHZ(1.26VCORE) 1.300V->0.990V (CPU SPEC: 1.260V -> 0.980V)

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

ROUTE AS DIFFERENTIAL PAIR

Fmax Test Connections

NO STUFF J7 M-ST-SM-52465-1217

1	VCORE_GNDDIV_TEST	12	VCORE_D0
2		11	VCORE_D1
3	VCORE_GNDSNS_TEST	10	VCORE_D2
4	+3V_PMU_RESET	9	VCORE_D3
5	SOFT_PWR_ON_L	8	VCORE_D4
6	NC (RFU)	7	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L71	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2493	1	RES,MF,1/16W,2.49K OHM,1%,0402,SMD	R93	?	CPU_BTR
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BTR
116S1000	1	RES,MF,1/16W,0 OHM,5%,0402,SMD	R93	?	CPU_BST_VCORE126
114S1503	1	RES,MF,1/16W,1.5K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE126

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VCORE SUPPLY

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1.5V/2.5V SWITCHER

M11 Power Shut down Sequencing

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
DDR RAM	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK CPU UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT CPUFB OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M11 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 37 OF 46	

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS0	CPU_AACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200	MIL7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800	MIL7		(250)			
	CPU_OACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_OREQ_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000	MIL7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100	MIL7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

TMDS/DVO SIGNAL CONSTRAINTS

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS
SI_TMDS_DN<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS
SI_TMDS_DP<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS
SI_TMDS_DN<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS
SI_TMDS_DP<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS
SI_TMDS_DN<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS
SI_TMDS_DP<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS
SI_TMDS_DN<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS
SI_TMDS_DP<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS
SI_TMDS_DN<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS
SI_TMDS_DP<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS
SI_TMDS_DN<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS
SI_TMDS_DP<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<23..0>	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610		
ATI_DVOD_DE	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_HSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_VSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:500 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R1	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R2	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	

TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS

GPU_R	GPU_R	500.0000	100 OHM SPACING
GPU_G	GPU_G	500.0000	100 OHM SPACING
GPU_B	GPU_B	500.0000	100 OHM SPACING

SIGNAL CONSTRAINTS - PAGE 1

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT	OF
NONE	38	46

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Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710				(200)		100 MHZ
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL				(200)		100.0 MHZ
	UIDE_DATA<6..0>	L:S::600				(200)		100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_DIOW_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING		(200)		100.0 MHZ
	UIDE_DMACK_L	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_CS0_L	L:S::500 MIL				(200)		100.0 MHZ
	UIDE_CS1_L	L:S::500 MIL				(200)		100.0 MHZ
	UIDE_DMARQ	L:S::400 MIL				(200)		100.0 MHZ
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING		(200)		100.0 MHZ
	UIDE_INTRQ	L:S::400 MIL				(200)		100.0 MHZ
	HD_DATA<15..0>	L:S:5000:6500	7			(200)		100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7			(200)		100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ
	HD_DIOW_L	L:S:3000 MIL:5200 MIL				(200)		100.0 MHZ
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING		(200)		100.0 MHZ
	HD_DMACK_L	L:S:4500 MIL:6000 MIL				(200)		100.0 MHZ
	HD_CS0_L	L:S:3000 MIL:6000 MIL				(200)		100.0 MHZ
	HD_CS1_L	L:S:3000 MIL:6000 MIL				(200)		100.0 MHZ
	HD_DMARQ	L:S:4500 MIL:6000 MIL				(200)		100.0 MHZ
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING		(200)		100.0 MHZ
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ
	EIDE_INT	L:S::500 MIL						33.00 MHZ
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_N	USB_TPAD_N	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_P	USB_TPAD_P	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	REMOVE CONSTRAIN TO AVOID DRC OCCUR					
	1772_CSSN					
	1772_CSSP					
	1772_CSIN					
	1772_CSIP					
	3V_SNSM					
	3V_SNSP					
	5V_SNSM					
	5V_SNSP					
	THERM1_M_DM					
	THERM1_M_DP					
	THERM2_M_DM					
	THERM2_M_DP					
	THERM1_A_DM					
	THERM1_A_DP					
	THERM2_A_DM					
	THERM2_A_DP					

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 39 OF 46	

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+BATT	VOLTAGE=12.8V	MIN_LINE_WIDTH=10MIL	MIN_NECK_WIDTH=25MIL
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 24 41
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 41
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 41
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 33 41
	I496 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 40
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 40
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 41
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 41
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	27 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	41
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	24 41
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23 41
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23 41
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 23 41
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 23
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10 23 41
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	23
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	23
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	23 41
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	23 41
AUDIO	I435 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 34
	I435 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 34
	I435 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50	27
FAN	I438 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27 41
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41

I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 IN
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 IN

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 35 41
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 7 8 15 16 35
	I386 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	I386 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	11
INTREPID	I383 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 41
CARDBUS	I386 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 19 21 41
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 19 21 22
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 22
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 19 22
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 19 20 21 22
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 15 16 19 21 22
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21 22
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 22
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
	I346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	I347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	21
	I348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10	36
	I349 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	21
	I350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	21
	I351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10	21
	I352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	21
	I353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	36
	I354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	36
	I355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	36
	I356 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 22
	I361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	I318 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
	I317 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 17
FW	I432 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=10 29
	I414 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 29 30
	I416 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30 41
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30 41
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I418 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	I386 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	33
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 33
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10	33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	36
	2_5V_ILIM		MIN_LINE_WIDTH=8	36
	MAX1715_TON		MIN_LINE_WIDTH=8	36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10 35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 35
	VCORE_ILIM		MIN_LINE_WIDTH=8	35
	VCORE_REF		MIN_LINE_WIDTH=8	35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	35
	VCORE_CC		MIN_LINE_WIDTH=8	35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	35 41
	VCORE_TIME		MIN_LINE_WIDTH=8	35
	VCORE_VGATE		MIN_LINE_WIDTH=8	14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	35
	I437 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10	35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 21
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 21
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 21
	1778_ION		MIN_LINE_WIDTH=8	21
	1778_ITH		MIN_LINE_WIDTH=8	21
	1778_ITH_RC		MIN_LINE_WIDTH=8	21
	1778_VFB		MIN_LINE_WIDTH=8	21 41
	1778_FCB		MIN_LINE_WIDTH=8	21
	1778_VRNG		MIN_LINE_WIDTH=8	21
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 36
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 36
	1_8V_VFB		MIN_LINE_WIDTH=8	36
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	36
	LTC3411_ITH		MIN_LINE_WIDTH=8	36
	LTC3411_SYNC		MIN_LINE_WIDTH=8	36
	LTC3411_SHDN		MIN_LINE_WIDTH=8	36
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 14
CY28512D LMU CONN	I436 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	I436 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 24
OPT DRIVER	I436 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 26

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SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE: NONE	SHT 40 OF 46	

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FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 28
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			28
	J4 JTAG_ASIC_TCK	TRUE			13 28
	J6 JTAG_ASIC_TRST_L	TRUE			13 28
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 24
	J14 INT_I2C_DATA0	TRUE			6 11 13 24
	J16 INT_I2C_CLK1	TRUE			13 14 24 25 27
	J17 INT_I2C_DATA1	TRUE			13 14 24 25 27
PWR/GND	J21 +PBUS	TRUE			40
	J21 +24V_PBUS	TRUE			40
	J25 GPU_VCORE	TRUE			19 21 40
	J24 1778_VFB	TRUE			21 40
	J27 CPU_VCORE_SLEEP	TRUE			5 6 35 40
	J26 VCORE_FB	TRUE			35 40
	J21 +1_8V_MAIN	TRUE			40
	J21 +2_5V_MAIN	TRUE			40
	J21 +5V_MAIN	TRUE	2		40 41
	J22 +5V_SLEEP	TRUE	2		40 41
	J22 +3V_MAIN	TRUE	4		24 40
		TRUE		1000	IN
	J22 +3V_PMU	TRUE			40
CARDBUS DVI	J36 CBUS_DET_1_L	TRUE		2000	18
	J35 CBUS_DET_2_L	TRUE		2000	18
	J40 TMDS_CONN_CLKN	TRUE		1000	23 38
	J39 TMDS_CONN_CLKP	TRUE		1000	23 38
	J42 VGA_R	TRUE		1000	23
	J41 VGA_G	TRUE		1000	23
	J44 VGA_B	TRUE		1000	23
	J43 VGA_HSYNC	TRUE		1000	23
	J46 VGA_VSYNC	TRUE		1000	23
	J45 DVI_DDC_CLK_UF	TRUE		1000	23
	J47 DVI_DDC_DATA_UF	TRUE		1000	23
	J48 DVI_HPD_UF	TRUE		1000	23
	J49 +5V_DDC_SLEEP	TRUE		2000	23 40
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	J52 LVDS_L0N			1000	21 23 39
	J51 LVDS_L0P			1000	21 23 39
	J53 LVDS_L1N			1000	21 23 39
	J55 LVDS_L1P			1000	21 23 39
	J54 LVDS_L2N			1000	21 23 39
	J57 LVDS_L2P			1000	21 23 39
	J56 CLKLVDS_LN	TRUE		1000	21 23 39
	J58 CLKLVDS_LP	TRUE		1000	21 23 39
	J59 LVDS_DDC_CLK	TRUE		1000	21 23
	J60 LVDS_DDC_DATA	TRUE		1000	21 23
	J62 +3V_LCD	TRUE	2	2000	23 40
	J22 +3V_SLEEP	TRUE		2000	40 41
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	J67 +14V_INV	TRUE		2000	23 40
	J66 +5V_INV_SW	TRUE		2000	23 40
	J68 BRIGHT_PWM	TRUE		2000	23
	J24 INV_GND	TRUE		2000	23
		TRUE		1000	IN
S-VIDEO	J70 TV_C	TRUE		2000	23
	J72 TV_Y	TRUE		2000	23
	J71 TV_COMP	TRUE		2000	23
	J73 TV_GND1	TRUE		2000	23 40
	J74 TV_GND2	TRUE		2000	23 40
LIO	J76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 27
	J75 INT_I2S0_SND_LRCLK	TRUE		1000	14 27
	J78 INT_I2S0_SND_MCLK	TRUE		1000	14 27 37
	J83 INT_I2S0_SND_SCLK	TRUE		1000	14 27
	J82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 27
	J77 SND_HP_MUTE_L	TRUE		1000	14 27
	J79 SND_AMP_MUTE	TRUE		1000	27
	J84 SND_HW_RESET_L	TRUE		1000	14 27
	J85 SND_HP_SENSE_L	TRUE		1000	14 27
	J86 SND_LIN_SENSE_L	TRUE		1000	14 27
	J81 INT_I2C_CLK2	TRUE		1000	14 27
	J80 INT_I2C_DATA2	TRUE		1000	14 27
	J87 ADAPTER_DET	TRUE		1000	27 31
	J88 CHARGE_LED_L	TRUE		1000	27 31
	J89 NEC_LUSB_OCI_UF	TRUE		1000	17 27
	J90 NEC_LUSB_PPON	TRUE		1000	17 27
	J22 +5V_MAIN	TRUE	2	2000	40 41
	J22 +5V_SLEEP	TRUE	2	3000	40 41
	J22 +3V_SLEEP	TRUE		2000	40 41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	J94 NEC_USB_DAM	TRUE			17 27 39
	J95 NEC_USB_DAP	TRUE			17 27 39
	J95 NEC_USB_DBM	TRUE			17 27 39
	J97 NEC_USB_DBP	TRUE			17 27 39
	J98 BT_USB_DM	TRUE			14 27 39
	J99 BT_USB_DP	TRUE			14 27 39
	J101 USB_TPAD_N	TRUE			14 24 39
	J100 USB_TPAD_P	TRUE			14 24 39
RT. USB WIRELESS	J102 NEC_RUSB_PPON	TRUE			17 27
	J103 NEC_RUSB_OCI_UF	TRUE			17 27
	J105 PCI_AD<0..31>	TRUE		1000	9 12 17 18 26 39
	J106 PCI_FRAME_L	TRUE		1000	12 17 18 26 39
	J108 PCI_TRDY_L	TRUE		1000	12 17 18 26 39
	J107 PCI_IRDY_L	TRUE		1000	12 17 18 26 39
	J109 PCI_DEVSEL_L	TRUE		1000	12 17 18 26 39
	J110 PCI_STOP_L	TRUE		1000	12 17 18 26 39
	J111 PCI_PAR	TRUE		1000	12 17 18 26 39
	J113 AIRPORT_PCI_REQ_L	TRUE		1000	12 26
	J112 AIRPORT_PCI_GNT_L	TRUE		1000	12 26
	J114 AIRPORT_PCI_INT_L	TRUE		1000	14 26
	J115 MAIN_RESET_L	TRUE		1000	14 17 18 19 20 26 31
	J116 CLK33M_AIRPORT	TRUE		1000	12 26 37
	J118 PMU_PME_L	TRUE		1000	14 17 26 31
	J119 ROM_ONBOARD_CS_L	TRUE		1000	9
	J121 ROM_OE_L	TRUE		1000	9 12
	J122 ROM_CS_L	TRUE		1000	9 12
	J123 ROM_RW_L	TRUE		1000	9 12
	J227 RF_DISABLE_L	TRUE		1000	26
	J230 AIRPORT_CLKRUN_L	TRUE		1000	26
	J124 +3V_AIRPORT	TRUE	4	2000	40
		TRUE	6	1000	IN
OPTICAL	J126 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	26 39
	J127 EIDE_OPTICAL_DMA_RQ	TRUE		2000	26 39
	J128 EIDE_OPTICAL_READ_L	TRUE		2000	26 39
	J129 EIDE_OPTICAL_DMAACK_L	TRUE		2000	26 39
	J130 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	26 39
	J131 EIDE_OPTICAL_CS0_L	TRUE		2000	26 39
	J132 EIDE_OPTICAL_CS1_L	TRUE		2000	26 39
	J133 EIDE_OPTICAL_RST_L	TRUE		2000	26 39
	J134 EIDE_OPTICAL_WR_L	TRUE		2000	26 39
	J135 EIDE_OPTICAL_IOCHRDY	TRUE		2000	26 39
	J136 EIDE_OPTICAL_INT	TRUE		2000	26 39
TRACKPAD	J137 +5V_TPAD_SLEEP	TRUE		3000	40
	J138 TPAD_F_TXD	TRUE		3000	
	J139 TPAD_F_RXD	TRUE		3000	
MODEM/ SERIAL	J139 SOFT_PWR_ON_L	TRUE		3000	23 24 31 35
	J141 COMM_RESET_L	TRUE		4000	14 27
	J140 COMM_SHUTDOWN	TRUE		4000	
	J142 COMM_RING_DET_L	TRUE		4000	14 27 31
	J143 COMM_TXD_L	TRUE		4000	14 27
	J144 COMM_TRXC	TRUE		4000	14 27
	J145 COMM_GPIO_L	TRUE		4000	14 27
	J146 COMM_DTR_L	TRUE		4000	14 27
	J147 COMM_RTS_L	TRUE		4000	14 27
	J148 COMM_RXD	TRUE		4000	14 27
KEYBOARD	J149 KBD_ID	TRUE		3000	24 31
	J150 KBD_INTL	TRUE		3000	
	J151 KBD_JIS	TRUE		3000	
	J152 KBD_CAPSLOCK_LED	TRUE		3000	
	J153 KBD_NUMLOCK_LED	TRUE		3000	
	J154 KBD_FUNCTION_L			3000	24 31
	J155 KBD_COMMAND_L			3000	24 31
	J156 KBD_OPTION_L			3000	24 31
	J157 KBD_CONTROL_L			3000	24 31
	J158 KBD_SHIFT_L			3000	24 31
	J159 KBD_X<0..9>			3000	24 31
	J160 KBD_Y<0..7>	TRUE		3000	
BATTERY	J161 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	J162 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	J163 BATT_CLK	TRUE		1000	32
	J164 BATT_DATA	TRUE		1000	32
	J165 PMU_BATT_DET_L	TRUE		1000	31 32
FANS	J167 +FAN_PWR	TRUE		3000	27 40
	J168 FAN1_TACH	TRUE		3000	27
	J169 FAN2_TACH	TRUE		3000	27
	J170 FAN1_GND	TRUE		3000	40
	J171 FAN2_GND	TRUE		3000	40
ETHERNET	J172 MDI_P<0..3>	TRUE		1000	28 39
	J173 MDI_M<0..3>	TRUE		1000	28 39
FIREWIRE	J174 FW_TPO0P	TRUE		1000	29 30 39
	J175 FW_TPO0N	TRUE		1000	29 30 39
	J176 FW_TPO0R	TRUE		1000	30
	J177 FW_TPI0P	TRUE		1000	29 30 39
	J178 FW_TPI0N	TRUE		1000	29 30 39
	J179 +FW_VP0	TRUE		1000	30 40
	J180 FW_VGND	TRUE		1000	41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	J181 FW_TPO1P	TRUE		1000	30 39
	J182 FW_TPO1N	TRUE		1000	30 39
	J183 FW_TPI1P	TRUE		1000	30 39
	J184 FW_TPI1N	TRUE		1000	30 39
	J185 +FW_VP1	TRUE		1000	30 40
	J186 FW_VGND	TRUE		1000	41
DC PWR IN	J187 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	32 33 40
LMU/ALS	J285 ST7_SLEEP_LED_H	TRUE			24
	J286 PMU_SLEEP_LED	TRUE			24
	J284 PMU_LID_CLOSED_L	TRUE			24 31
	J282 LMU_DETECT	TRUE			24
		TRUE	6	1000	IN
MISC.	J192 SLEEP_LED	TRUE	(100 MIL PROBE PREFERRED)		24
	J193 PMU_KB_RESET_L	TRUE			
	J194 SLEEP	TRUE			24 27 31 34 36
	J195 PMU_CPU_HRESET_L	TRUE			6 31
	J196 BB_RESET_L	TRUE			6
	J224 +3V_PMU_RESET	TRUE			31 35
	J225 MMM_ACC_X_AXIS	TRUE			25
	J226 MMM_ACC_Y_AXIS	TRUE			25
	J200 MMM_ACC_Z_AXIS	TRUE			25
	J267 MMM_ACC_SELFTEST	TRUE			25
	J258 +BATT_ISNS_P	TRUE			25
	J259 +PPBATT_ISNS_N	TRUE			25
	J260 +PWR_SUPERCAP	TRUE			33
	REMOVE CONSTRAIN FOR UNUSED FUNCTIONAL TP				
	J281 +3V_HALL_EFFECT				24 40
	J283 LID_CLOSED_L				24
	J285 TMDS_DN<0..2>				20 23 39
	J286 TMDS_DP<0..2>				20 23 39

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REVISION HISTORY

EVT2 RELEASE

08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH
2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462)
3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2
4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT
5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING

08/16/04 - 1. MODIFY CPU_AVDD SETTING
08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT
09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES
09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN
2. MODIFY CPU_AVDD SEETING AGAIN
3. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM
09/03/04 - 1. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802
2. ADD R803 BETWEEN DP6 AND DCDC_IN
3. ADD R804 AND SUPERCAP C692 ON +4_6V_BU
4. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT

09/06/04 - 1. ADD EMI SOLUTION L12
09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT
09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT
09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT
09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT
2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU
09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33
2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR

DVT RELEASE

09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT
10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT
10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR
10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467
11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313

PVT RELEASE

12/17/04 - 1. REMOVE ALL OPEN JUMPER
12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL 28D2< 40B3>
+1_5V_AGP 12B5< 12D1< 12D4< 15D6< 16C8<
19C6< 19D6< 21A8< 21B4<> 21D5<>
22B8< 22D6< 40C3>
+1_5V_AGP_GPU 22C5< 40C3>
+1_5V_AGP_NECK 21B4<> 40B3>
+1_5V_GPU_VDD15 21D3< 40C3>
+1_5V_INTREPID_PLL 8D6< 12D4< 12D8< 14D6<> 40D3>
+1_5V_INTREPID_PLL1 14C3< 40D3>
+1_5V_INTREPID_PLL2 14D3< 40D3>
+1_5V_INTREPID_PLL3 14D3< 40D3>
+1_5V_INTREPID_PLL4 14D3< 40D3>
+1_5V_INTREPID_PLL5 12D3< 40D3>
+1_5V_INTREPID_PLL6 12D6< 40D3>
+1_5V_INTREPID_PLL7 8D5< 40D3>
+1_5V_INTREPID_PLL8 14D3< 40C3>
+1_5V_LDO 40D6>
+1_5V_MAIN 40D6>
+1_5V_SLEEP 40D6>
+1_5V_SLEEP_NECK 36D2<> 40B3>
+1_5V_SLEEP_VIN 40D6>
+1_8V_ATI_PVDD 21C5<> 22B6< 22B6< 22D6<> 40C3>
+1_8V_ATI_TPVDD 22D2<> 40B3>
+1_8V_GPU 19A8< 20A6< 21D7< 22A2< 22A6<
22B1< 22B6< 22C8< 22D6< 22D8< 40C3>
+1_8V_GPU_AVDD 22D5< 40B3>
+1_8V_GPU_AVDDQ 22D4< 22D7< 40B3>
+1_8V_GPU_DVO 22B2<
+1_8V_GPU_MEMPLL 22B5< 40B3>
+1_8V_GPU_PLL 22D5< 40C3>
+1_8V_GPU_PNLIO 22A5< 40B3>
+1_8V_GPU_PNLPLL 22B5< 40B3>
+1_8V_GPU_TP_PLL 22B5< 22D1< 40B3>
+1_8V_GPU_VDDDI 22C7< 22D4< 40C3>
+1_8V_MAIN 40D6> 41C6>
+1_8V_PVDD_NECK 21B5<> 40B3>
+1_8V_SLEEP 40D6>
+1_8V_SLEEP_NECK 36D2<> 40B3>
+1_95V_FW_DVDD 29C4< 29C7<> 29D5< 40A3>
+1_95V_FW_DVDD_PORT1 29D6< 40A3>
+1_95V_FW_DVDD_RX0 29C5< 40A3>
+1_95V_FW_DVDD_TX0 29C5< 40A3>
+1_95V_FW_PLL400VDD 29C4< 40A3>
+1_95V_FW_PLL500VDD 29D4< 40A3>
+1_95V_FW_PLLVDD 29D4< 29D6<> 40A3>
+2_5V_CG_MAIN 14C6<
+2_5V_GPU 22A7<> 40C3>
+2_5V_GPU_A2VDD 22D4< 22D7< 40B3>
+2_5V_GPU_MCLK 22C7< 22D4< 40B3>
+2_5V_GPU_MEMCORE 22C5< 40C3>
+2_5V_GPU_PNLIO 22A5< 40C3>
+2_5V_INTREPID 9A7< 10D3< 10D5< 10D6< 10D8< 15D6<
16B8< 40D3>
+2_5V_MAIN 40D6> 41C6>
+2_5V_MARVELL 28B8< 28C4< 40B3>
+2_5V_MARVELL_AVDD 28C4< 40B3>
+2_5V_MARVELL_CONN 28B3<>
+2_5V_REG 30A6<
+2_5V_REG_F 30A7<>
+2_5V_SLEEP 40D6>
+2_5V_SLEEP_NECK1 21C4<> 40B3>
+2_5V_SLEEP_NECK2 36D2<> 40B3>
+3V_AIRPORT 40C3> 41C3>
+3V_ATI_OSC_SLEEP 19B2< 40B3>
+3V_ATI_SS 19A3< 40B3>
+3V_CG_PLL_MAIN 14C6<
+3V_FW 29A3< 29D7<> 30B7<> 30D5< 40A3>
+3V_FW_AVDD 29C6< 40A3>
+3V_FW_AVDD_PORT0 29C6< 40A3>
+3V_FW_AVDD_PORT1 29C6< 40A3>
+3V_FW_AVDD_PORT2 29D6< 40A3>
+3V_FW_ESD 30A5< 30B4<> 30D3<>
+3V_FW_ESD_ILIM 30D4<
+3V_FW_ESD_R 30A6<
+3V_FW_UF 29D7<> 40A3>
+3V_GPU 12D1< 19B8< 19C6< 19C8< 19D6<
21C4< 21C5< 21C7< 21D7< 22A6< 22B1<
40C3>
+3V_GPU_FLT 22B2< 40C3>
+3V_HALL_EFFECT 24B2<> 40B6> 41C1>
+3V_INTREPID_USB 14C3< 40D3>
+3V_LCD 23B4<> 40B6> 41B6>
+3V_LCD_SW 23B4<> 40B6>
+3V_MAIN 24B8<> 40D6> 41C6>
+3V_MAIN_AUD 27C6<> 34C1<> 40B6>
+3V_MAIN_JUMPER 34D2<> 40D1>
+3V_MAIN_LMU 24D7<> 40A1>
+3V_MAIN_SSCG 40A1>
+3V_NEC_VDD 17B3< 17D7< 17D7< 40A3>
+3V_PMU 40D6> 41C6>
+3V_PMU_AVCC 27B1< 31B6< 31D5<> 40C6>
+3V_PMU_ESR 33A2< 40C6>
+3V_PMU_RESET 31C7< 35A4<> 41C1>
+3V_SENSOR 24B4<>
+3V_SLEEP 40D6> 41A6> 41B6>
+3V_SLEEP_NECK 36D1<> 40B3>
+3V_SLEEP_PCCARD 18D7< 40C3>
+3V_SLP_OK_L 34B4<>
+3V_SLP_ON 34A5<>
+4_6V_BU 33B3<> 34B7< 40C6>
+4_85V_ESR 33A4< 40C6>
+4_85V_RAW 31A4< 33B4<> 40C6>
+5V_DDC_SLEEP 23D3<> 23D5<> 40B6> 41B6>
+5V_DDC_SLEEP_UF 23D6< 40B6>
+5V_HDD 26D1<>
+5V_HD_SLEEP 26D1<> 34A7<> 40C6>
+5V_INV_SW 23B2<> 40B6> 41A6>
+5V_INV_UF_SW 23B2<> 40B6>
+5V_MAIN 40D6> 41A6> 41C6>
+5V_MAIN_AUD 27C6<> 34C8<> 40B6>
+5V_MAIN_JUMPER 34D8<> 40D1>
+5V_SLEEP 40D6> 41A6> 41C6>
+5V_SLEEP_LMU 24C6<> 24C7<>
+5V_SLEEP_OPT 26B5<> 40A1>
+5V_TPAD 24B5<>
+5V_TPAD_FB 24B4<>
+5V_TPAD_SLEEP 40B6> 41B3>
+14V_INV 23B2<> 40B6> 41B6>
+24V_PBUS 40D6> 41C6>
+ADAPTER 32D8<> 33A7< 40C6> 41D1>
+ADAPTER_ILIM 33A6<> 40C6>
+ADAPTER_OR_BATT 33A5<> 40C6>
+ADAPTER_SENSE 32D4<> 40C6>
+ADAPTER_SW 32D5<> 40C6> 40C6>
+BATT 40D6>
+BATT_14V_FUSE 32D1<> 40C6>
+BATT_24V_FUSE 32B1< 32D2<> 40C6>
+BATT_ISNS_P 25A5<> 41C1>
+BATT_POS 32A4<> 40C6> 41A3>
+BATT_RSNS 32B2< 40C6>
+BATT_VSNS 32A4< 40C6>
+FAN_PWR 27A3< 27A4< 40B6> 41A3>
+FW_AMP_SENSE 40A3>
+FW_PBUS 30D7<> 40A3>
+FW_PWR1 30B5< 40A3>
+FW_PWR_CTRL 30A7<>
+FW_PWR_OR 29B8< 29D8<> 30D5<> 40A3>
+FW_PWR_OR_F 30B7<>
+FW_PWR_OR_GATE 30B8<>
+FW_PWR_OR_GATE_L 30A8<
+FW_SW 30D5<> 40A3>
+FW_VP0 30C1<> 40A3> 41A3>
+FW_VP1 30A3<> 40A3> 41D1>
+GPU_VDD15_NECK 21B5<> 40B3>
+GPU_VDD15_UF 21B5<> 21D4<> 40B3>
+HD_LOGIC_SLEEP 26C2<> 40C6>
+PBUS 40D6> 41C6>
+PBUS_JUMPER 33C3<> 40D1>
+PPBATT_ISNS_N 25A4<> 41C1>
+PWR_SUPERCAP 33A4< 41C1>
+VCC_CBUS_SW 18B1< 18B2< 18D2<> 40C3>
+VPP_CBUS_SW 18B1< 18B2< 18D2<> 40C3>
1V20_REF 32C7< 33C8< 40D1>
1V65_REF 32A5<
1_5V_BOOST 36C6<> 40C1>
1_5V_BST 36C5<> 40C1>
1_5V_DH 36C5<> 40C1>
1_5V_DL 36B5<> 40C1>
1_5V_FB 36B5< 36B7< 40C1>
1_5V_ILIM 36C5<> 40C1>
1_5V_LX 36B5<> 40C1>
1_5V_LX_F 36B7<> 36C5<> 40C1>
1_5V_SLEEP_EN_L 36C7<> 36D7<>
1_8V_PVDD_STD 22D6<
1_8V_SLEEP_PWREN_L 36A3<>
1_8V_SW 36A5<> 40A1>

1_8V_SW_F 36A4<> 40A1>
1_8V_TPVDD_STD 22D1<
1_8V_VFB 36A5<> 40A1>
2_5V_BOOST 36C4<> 40D1>
2_5V_BST 36C4<> 40D1>
2_5V_DH 36C3<> 40D1>
2_5V_DL 36B3<> 40C1>
2_5V_FB 36B4<
2_5V_ILIM 36C5<> 40C1>
2_5V_LX 36B3<> 40D1>
2_5V_LX_F 36B2<> 36C4<> 40D1>
2_5V_SLEEP_PWREN_L 36C2<>
3V_5V_OK 24A6<> 34B4<> 36A8<> 36D6<>
3V_5V_OK_G 24A6<
3V_5V_OK_L 24B5<>
3V_BG 34C4<>
3V_BOOST 34C4<>
3V_BOOST_ESR 34D3<>
3V_ITH 34C4<>
3V_ITH_RC 34C3<
3V_PMU_VTAP 33B3<
3V_RSNS 34D2< 40D1>
3V_RUNSS 34C4<
3V_SLEEP_PWREN_L 34B3<>
3V_SNSM 34C4< 39A2>
3V_SNSP 34C4< 39A2>
3V_SW 34C4<> 40D1>
3V_TG 34D4<>
3V_VOSNS 34C4<>
5V_BG 34C5<>
5V_BOOST 34C5<>
5V_BOOST_ESR 34D6<>
5V_HD_PWREN 34A8<>
5V_ITH 34C5<>
5V_ITH_RC 34C6<
5V_RSNS 34D7< 40D1>
5V_RUNSS 34C5<
5V_SLEEP_PWREN 34A8<>
5V_SNSM 34C5< 39A2>
5V_SNSP 34C5< 39A2>
5V_SW 34C5<> 40D1>
5V_TG 34C5<>
5V_VOSNS 34C5<>
1625_BG 33C5<>
1625_BST 33C5<
1625_BST_ESR 33C5<>
1625_COMP 32D2< 33C6<
1625_DIV 33C8<
1625_ENABLE 33D7<>
1625_ENABLE_L 33D6<>
1625_EXTVCC 33D5<> 40D1>
1625_FCB 33C6<
1625_INTVCC 33C5<> 40D1>
1625_RUNSS 33C6<
1625_SGND 33B7<> 40D1>
1625_TG 33C5<>
1625_VFB 33B5<>
1625_VIN 33C6< 40D1>
1625_VSW 33C4<> 40D1>
1772_ACIN 32B5<
1772_ACOK_L 32B5<> 32C4<>
1772_BST 32B4<>
1772_BST_ESR 32C3<
1772_CCI 32B5<>
1772_CCS 32B5<
1772_CCV 32B5<>
1772_CCV_RC 32B5<
1772_CELLS 32B4<
1772_CLS 32A4<
1772_CSIN 32B4<> 39A2>
1772_CSIP 32B4<> 39A2>
1772_CSSN 32C5< 39A2>
1772_CSSP 32C5< 39A2>
1772_DCIN 32B5< 40C6>
1772_DHI 32B4<>
1772_DLO 32B4<>
1772_DLOV 32B4<> 40C6>
1772_GND 32A5<> 40C6>
1772_ICHG 32B5<>
1772_ICTL 32B5<>
1772_IINP 32B5<
1772_LDO 32C4<> 40C6>
1772_LX 32B4<> 40C6>
1772_REF 32B5<>
1772_VCTL 32B5<
1778_BG 21A5<> 40B1>
1778_BST 21A5<> 40B1>
1778_BST_RC 21A5< 40B1>
1778_FCB 21A6< 40B1>
1778_GND 21A6< 21A7<> 40B1>
1778_ION 21A5< 40B1>
1778_ITH 21A6<> 40B1>
1778_ITH_RC 21A7< 40B1>
1778_SHDN_L 21A6<>
1778_TG 21A5<> 40B1>
1778_VCC 21A5< 40B1>
1778_VFB 21A2< 21A5< 40B1> 41C6>
1778_VIN 21A5< 40B1>
1778_VRNG 21A6< 40B1>
3405_MODE 28D5<
3405_VFB 28D4<>
3707_FCB 34C5<
3707_FSET 34C5<
3707_INTVCC 34D4<> 40D1>
3707_SGND 34B5<> 40D1>
3707_STBY 34C5<>
A29_CLS_ADJ 32A5<>
A29_CURRENT_ADJ 32C4<>
A29_DETECT 31A2< 32A5<> 32C4<>
A29_DET_L 31A3<
A29_DET_REF 31A4<
AC_DET 31A4<
AC_DIV 32C7<
AC_ENABLE_GATE 32D6<>
AC_ENABLE_L 32C5<>
AC_GTR_18V 32C3<>
AC_IN 28B8<> 30C8< 31B3< 32C5<> 32C6<>
AC_IN_FW_CNTL 30C7<>
AC_IN_L 31A8<> 32C2<> 32C6<>
AC_IN_L_RC 32C2<>
ADAPTER_DET 27D8<> 31A4< 41A6>
ADAPTER_I_REG 32D3<>
ADT7467_ADR_ENABLE_L 27B3<>
ADT7467_TACH3_TP 27B3<
ADT7467_THERM_L 24B4<> 27A2<> 27B3<
ADT7467_VCC 27C4<
ADT7467_VCORE_MON 5C8<> 27B4<
AGP8X_DET_PU 19C6<>
AGP_AD<0> 12D2<> 19C7<>
AGP_AD<15..0> 39D5>
AGP_AD<1> 12C2<> 19C7<>
AGP_AD<2> 12C2<> 19C7<>
AGP_AD<3> 12C2<> 19C7<>
AGP_AD<4> 12C2<> 19C7<>
AGP_AD<5> 12C2<> 19C7<>
AGP_AD<6> 12C2<> 19C7<>
AGP_AD<7> 12C2<> 19C7<>
AGP_AD<8> 12C2<> 19C7<>
AGP_AD<9> 12C2<> 19C7<>
AGP_AD<10> 12C2<> 19C7<>
AGP_AD<11> 12C2<> 19C7<>
AGP_AD<12> 12C2<> 19C7<>
AGP_AD<13> 12C2<> 19C7<>
AGP_AD<14> 12C2<> 19C7<>
AGP_AD<15> 12C2<> 19C7<>
AGP_AD<16> 12C2<> 19C7<>
AGP_AD<31..16> 39D5>
AGP_AD<17> 12C2<> 19C7<>
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CPU_VCORE_SEQ 35D8<
CPU_VCORE_SEQ_L 35D8<
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41C6>
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CSLOT_ADDR4_SPN 13B7>
CSLOT_ADDR5_SPN 13B7>
CSLOT_ADDR6_SPN 13B7>
CSLOT_ADDR7_SPN 13B7>
CSLOT_ADDR8_SPN 13B7>
CSLOT_ADDR9_SPN 13B7>
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CSLOT_CE2_L_SPN 13C7>
CSLOT_IORD_L_SPN 13C7>
CSLOT_IOWAIT_L_PU 13C7<
CSLOT_IOWR_L_SPN 13C7>
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DCDC_EN_L 34B6< 34B7<> 36C7<>
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DVI_DDC_CLK_UF 23C5<> 23D3<> 41B6>
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DVI_DDC_DATA_UF 23C5<> 41B6>
DVI_HPD 23C4<>
DVI_HPD_DIV 23C2<
DVI_HPD_UF 23C3< 23C5<> 41B6>
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EIDE_OPTICAL_CS1_L 26A6<> 26A7< 39B5> 41C3>
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EIDE_OPTICAL_WR_L 26A5<> 26A7< 39B5> 41B3>
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EIDE_WR_L 13A7> 26A8< 39B5>
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ENET_CRS 13C5< 28B7> 39A5>
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ENET_RST_L 28B7<
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ENET_RX_ER 13C5< 28B7> 39A5>
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FAN1_PWM_L 27A5<> 27B2<>
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FW_TPO0P 29B2<> 30C3<> 39D2> 41A3>
FW_TPO0R 30C1<> 41A3>
FW_TPO1N 30A3<> 39D2> 41D1>
FW_TPO1P 30A3<> 39D2> 41D1>
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FW_XI 29A4<> 37A1>
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GPU_C 21D6<> 23A8<
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GPU_R 21D6<> 23B8< 38B1>
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GPU_VCORE_SEQ 21A8<
GPU_VCORE_SEQ_L 21A8<
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HD_CS1_L 26B3< 26C1<> 39B5>
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HD_DIOW_L 26A3< 26C1<> 39B5>
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HD_DMARQ 13C6< 26C2<> 39B5>
HD_INTRQ 13C6< 26C1<> 39B5>
HD_IOCHRDY 26A3< 26C1<> 39B5>
HD_RESET_L 26A3< 26D2<> 39C5>
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IAC_RC_COMP 32D3<
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13C3<> 24D7<> 41C6>
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27B4< 41C6>
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INT_I2C_DATA1 13B2< 13C3<> 14B7< 24B3<> 25C2<>
27B4<> 41C6>
INT_I2C_DATA2 14A2<> 27D7<> 41A6>
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INT_I2S0_SND_SCLK 14B1< 27D7<> 41A6>
INT_I2S0_SND_SCLK_UF 14A3<>
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INT_I2S0_SND_TO_DAC_UF 14B3<>
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INT_MEM_VREF 9A7< 9B6<> 40C3>
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INT_TST_MONOUT_TP 13C5> 41C6>
INT_TST_PLLEN_PD 13C5< 13D2< 41C6>
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INV_ON_PWM 21C6<> 23A3<

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JTAG_ASIC_TMS 13C5< 13D2< 28A5< 41D6>
JTAG_ASIC_TRST_L 13C2< 13C5< 28A5< 41D6>
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JTAG_CPU_TDI 5B2< 5C3< 6B2<> 41D6>
JTAG_CPU_TDO_TP 5C3> 41D6>
JTAG_CPU_TMS 5B2< 5B3< 6B2<> 41D6>
JTAG_CPU_TRST_L 5B3< 6A4< 6B2<> 41D6>
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KBDLED_RETURN 24B3<> 24D7<>
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KBD_COMMAND_L 24C2< 31C6<> 41B3>
KBD_CONTROL_L 24C2< 31C6<> 41A3>
KBD_FUNCTION_L 24C2< 31B6<> 41B3>
KBD_ID 24D2< 31B6<> 41B3>
KBD_INTL 41B3>
KBD_JIS 41B3>
KBD_NUMLOCK_LED 41B3>
KBD_OPTION_L 24C2< 31B6<> 41B3>
KBD_SHIFT_L 24C2< 31C6<> 41A3>
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KBD_Y<0..7> 41A3>
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LCD_PWREN_L 23B5<>
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LED_LINK100 28B5<>
LED_RX_SPN 28B5>
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LT1962_INT_BYP 14D7<>
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LTC1962_INT_VIN 14D8<> 40A1>
LTC3405_SW 28D4<> 40A3>
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LTC3411_ITH 36A5<> 40A1>
LTC3411_ITH_RC 36A5< 40A1>
LTC3411_SHDN 36A6<> 40A1>
LTC3411_SYNC 36A6<> 40A1>
LTC3411_VCC 36A6< 36A7< 40B1>
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LVDS_DDC_DATA 21C5<> 23A4< 23B4<> 41B6>
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LVDS_L0P 21B5> 23B4<> 39C2> 41B6>
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RAM_DATA_B<9>    10C8<> 11D5<>
RAM_DATA_B<10>   10C8<> 11D5<>
RAM_DATA_B<11>   10C8<> 11D5<>
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RAM_DATA_B<14>   10C8<> 11D3<>
RAM_DATA_B<15>   10C8<> 11D3<>
RAM_DATA_B<16>   10C6<> 11D5<>
RAM_DATA_B<23..16>  37C5>
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RAM_DATA_B<22>   10C6<> 11C3<>
RAM_DATA_B<23>   10C6<> 11C3<>
RAM_DATA_B<32>   10C4<> 11B5<>
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RAM_DATA_B<31>   10C6<> 11C3<>
RAM_DATA_B<32>   10B4<> 11B5<>
RAM_DATA_B<39..32>  37B5>
RAM_DATA_B<33>   10C4<> 11B5<>
RAM_DATA_B<34>   10C4<> 11B5<>
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RAM_DATA_B<36>   10C4<> 11B3<>
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RAM_DATA_B<40>   10C4<> 11B5<>
RAM_DATA_B<47..40>  37B5>
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RAM_DATA_B<55>   10C2<> 11A3<>
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RAM_DATA_B<63>   10C2<> 11A3<>
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RAM_DQM_A<1>     10C7<> 11D6<> 37C5>
RAM_DQM_A<2>     10B6<> 11C6<> 37C5>
RAM_DQM_A<3>     10C5<> 11C6<> 37C5>
RAM_DQM_A<4>     10B4<> 11B6<> 37B5>
RAM_DQM_A<5>     10C3<> 11B6<> 37B5>
RAM_DQM_A<6>     10B2<> 11A6<> 37B5>
RAM_DQM_A<7>     10C1<> 11A6<> 37A5>
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RAM_DQS_A<2>     10B6<> 11C8<> 37C5>
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RAM_WE_L         9A4< 11B5<> 11B8<> 37A5>
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ROM_ONBOARD_CS_TP_L  9B3< 26C6<>
ROM_RW_L         9B3< 12A4< 41C3>
ROM_RW_TP_L      9B3< 26C6<>
ROM_WP_L         9B3<
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SI_I2C_CLK       20B4< 20B7< 20D7< 21C5<>
SI_I2S_DATA      20B4<> 20B7<> 20D7< 21C5<>
SI_M_HTPLG       20B7<
SI_RESET_L       20B6< 21C7<>
SI_RESET_L_R     20B4< 20B7< 20D7<
SI_SECONDARY     20A8< 20D5<>
SI_S_HTPLG       20B4<
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SI_TMDS_DN<5>    20A2< 20A4< 38D1>
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SLEEP_LED_L      24D4<
SLEEP_LED_SW_L   24D4<>
SLEEP_LED_UF     24D3<
SLEEP_LS5        34A4<> 34A8<
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SLEEP_L_LS5_NET  34B3<> 36C8<>
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SND_AMP_MUTE     27C7<> 27D6<> 41A6>
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SND_AMP_MUTE_L   14B5<> 27D5<>
SND_HP_MUTE      27C5<>
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SND_HP_MUTE_LO   27C6<> 27C7<>
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SND_HW_RESET_L   14A8< 14B5<> 27D7<> 41A6>
SND_LIN_SENSE_L  14B5<> 27C8<> 41A6>
SOFTMODEM_FC_RGDT  27D3<
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                 35A4<> 41B3>
ST7_SLEEP_LED_H  24C5<> 24C6<> 24D6<> 41D1>
STOP_AGP_L       12D2< 12D4<>
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SYSCLK_CPU_UF    8A5<> 37D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 37C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37C1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 37D1>
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THERM1_DP        27A5< 27A6< 27B5<> 27B6< 39A2>
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THERM1_M_DP      27B7< 27B8< 39A2>
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TPAD_F_TXD       41B3>
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TPAD_TXD         31B2< 31C4<>
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TP_MMM_ICSP_PGD  25C3<>
TP_MMM_ICSP_PGM  25C3<>
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TV_GND2          23A6<> 40B6> 41A6>
TV_Y             23A6<> 41A6>
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UIDE_DIOW_L      13C7<> 26A4< 39C5>
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UIDE_DMARQ       13C7<> 39C5>
UIDE_INTRQ       13C7< 39C5>
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UIDE_RST_L       13C7<> 26A4< 39C5>
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USB_DDM          14B2<> 14C2<
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USB_DEP          14B2<> 14C2< 39B2>
USB_DFM          14B2<> 14B2< 39B2>
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USB_OC_EF_L      14B2< 14C7<
USB_PWREN_AB_L   14B2<> 14C7<
USB_PWREN_CD_L   14B2<> 14C7<
USB_PWREN_EF_L   14B2<> 14C7<
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USB_TPAD_P       14C1< 24B4<> 39B2> 41D3>
VCORE_AB_SEL     35A7<> 35C6<
VCORE_AB_SEL_INV  35A7<>
VCORE_AB_SEL_OPT  35A6<>
VCORE_BOOST      35C4<> 40C1>
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VCORE_DG         35A3<>
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VCORE_DH         35B5<> 40C1>
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VCORE_GND        35B5<> 40B1>
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VCORE_GNDDIV     35A5< 35A5< 40B1>
VCORE_GNDDIV_TEST  35A4<>
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VCORE_LX         35B5<> 40C1>
VCORE_OFFSET_DIV  35B6<>
VCORE_REF        35B6<> 40C1>
VCORE_SHDN_L     5B3< 35C6<>
VCORE_SHDN_L_3V  5B3<>
VCORE_SNS        35A1<> 40B1>
VCORE_TIME       35B4<> 40B1>
VCORE_TON        35B6< 40C1>
VCORE_VCC        35C6< 40C1>
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VCORE_VID<2>     35B7< 35D4<
VCORE_VID<3>     35B7< 35D4<
VCORE_VID<4>     35B7< 35D4<
VCORE_VSENSE     35C2<>
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VGA_HSYNC        23C6<> 23D7< 41B6>
VGA_R            23B6< 23C5<> 41B6>
VGA_VSYNC        23C5<> 23D7< 41B6>
ZT10_SPN         4C2<>
ZT301_SPN        4C2<>
ZT302_SPN        4C2<>
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SCALE: NONE	SHT 44 OF 46	

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*** Part Cross-Reference for the entire design ***

C1	CAP	5
C2	CAP	5
C3	CAP	35
C4	CAP	35
C5	CAP	35
C6	CAP	35
C7	CAP	34
C8	CAP	34
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J2	CON_4RT_WRIB	24
J3	CON_M40ST_D4MT_SM	27
J4	CON_4RT_WRIB	23
J5	CON_M80ST_D4MT_SM	18
J6	CON_F80ST_D4MT_SM	26
J7	CON_12	35
J8	CON_2RTSM_125	24
J9	CON_F1ST_S2MT_SM	14
J10	CON_M16ST_D_SMA	24
J12	CON_M50SM_5MM	26
J13	CON_M50SM_5MM	26
J14	CON_F30RT_S2MT_SM	23
J15	CON_F10RT_S2MT_SM	27
J16	CON_3RTSM_125	33
J17	CON_M16ST_D_SMA	27
J18	CON_M4RT_S2MT_SM	27
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J21	CON_F5RT_MINIDIN_TH	23
J22	CON_F30RT_T6MT_TH1	23
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J24	CON_F6RT_S4MT_TH1	30
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J26	CON_M8RT_S_SM	32
J27	CON_M4RT_S_SM	32
J28	CON_10STSM_5087	27
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RP36	RPAK4P	12
RP37	RPAK4P	29
RP38	RPAK4P	29
RP39	RPAK4P	31
RP40	RPAK10P2C	24

RP41	RPAK4P	31
RP42	RPAK10P2C	24
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP61	RPAK2P	20
RP70	RPAK2P	20
RP72	RPAK2P	20
RP74	RPAK2P	20
RP75	RPAK2P	20
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	32
U2	NC7S32	23
U3	AMP_MAX4172	32
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	32
U7	MAX1717	35
U8	PCI1510GGU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	33
U14	COMPARATOR_LMC7211	33
U15	PIC16F818_QFN	25
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	36
U20	KXM52	25
U21	741125	24
U22	VREG_LP2951	33
U23	VREG_LP2951	33
U24	SIL178	20
U25	SIL178	20
U26	MAX6804	31
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	31
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	21
U33	COMPARATOR_LMC7211	31
U34	VREG_MM1571J	22
U35	LTC3707	34
U36	TSB81BA3A	29
U37	VREG_LM2594	29
U38	VREG_LT1962	29
U39	741G32	23
U40	741G32	23
U41	INA138	25
U42	COMPARATOR_LMC7211	23
U43	TRANSCEIVER_88E1111	28
U44	LTC1761	29
U45	LTC3405	28
U46	LTC3411	36
U47	RAGE_MBLTY_M11_CSP64_667	19 21 22
U48	TRA_SI5467BDQ	36
U49	VREG_LT1962	14
U50	TRA_SI3447DV	36
U51	INTREPID 8 9 12 13 14 15	
U52	EEPROM_32KX8_M24256B	6
U53	ADT7467	27
U54	ATTINY2313	6
U55	OPAMP_LMC7111	32
U56	APOLLO_MPC7447A_360	5 6
U57	COMPARATOR_LMC7211	32
U58	LIS3L02AQ	25
U59	COMPARATOR_LMC7211	30
U60	VREG_MM1571J	22
XW1	SHORT	32
XW2	SHORT	35
XW3	SHORT	33
XW4	SHORT	21
XW5	SHORT	21
XW6	SHORT	21
XW7	JUMPER	21
XW8	SHORT	36
XW9	SHORT	21
XW10	SHORT	36
XW11	SHORT	21
XW12	SHORT	21
XW13	SHORT	34
XW14	SHORT	23
XW15	SHORT	23
XW16	JUMPER	22
XW17	SHORT	36
XW18	JUMPER	26
XW19	JUMPER	33
XW20	JUMPER	34
XW21	SHORT	36
XW22	JUMPER	34
XW23	SHORT	36
XW24	JUMPER	36
XW25	SHORT	36
XW26	JUMPER	36
XW27	SHORT	35
XW28	SHORT	35
XW29	SHORT	35
XW30	SHORT	27
XW31	SHORT	34
XW32	SHORT	34
XW33	JUMPER	36
XW34	SHORT	5
XW35	SHORT	25
XW36	SHORT	25
XW37	SHORT	25
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	31
Y4	CRYSTAL	31
Y5	CRYSTAL_4PIN	28
ZT1	HOLE_VIA	4
ZT2	HOLE_VIA	4
ZT3	HOLE_VIA	4
ZT4	HOLE_VIA	4
ZT5	HOLE_VIA	4
ZT6	HOLE_VIA	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	HOLE_VIA	4
ZT11	HOLE_VIA	4
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ZT13	HOLE_VIA	4
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ZT15	HOLE_VIA	4
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ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
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ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
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ZT82	HOLE_VIA	4
ZT83	HOLE_VIA	4
ZT84	HOLE_VIA	4
ZT85	HOLE_VIA	4
ZT86	HOLE_VIA	4

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